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for FrontIEr Research and Industry
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Parametric study of CMOS Photodetectors
Computer Aided Class

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Université Claude Bernard Lyon 1

Outline

- Introduction : Main objectives – Organization – CAD tool
- Class level 1: Light to silicon interaction
- Class level 2: CMOS photodiodes design
- Class level 3: Multi buried photodetectors
- Complements
- Conclusion - Debriefing

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Introduction

Main objectives
A parametric study of the main parameters used for CMOS photodiodes design

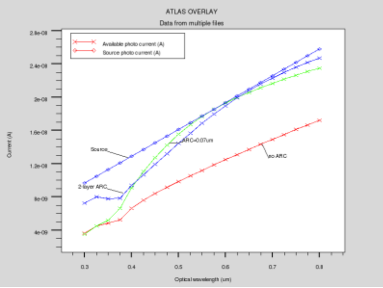
Organization
The class is organized in 3 sections. The concepts for each section are first introduced , followed by some simulations for concepts illustration and a reminder slide points out the key aspects of the studied section

CAD tool
It is an R&D and teaching Matlab tool (not a commercial one) developed by Paris 6 and Lyon 1 universities.
The 1D modeling is restricted to abrupt *pn* junction in silicon

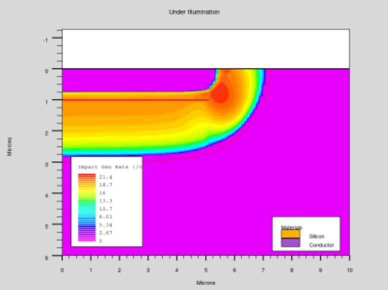
More realistic 1D, 2D, and 3D physical modeling could be performed with TCAD software (multiphysics process and device). CMOS photodiodes and associated front end electronics could be designed using CADENCE with foundry design kits with simulation tools such SPICE and SPECTRE

Introduction

TCAD : process and device simulation tools



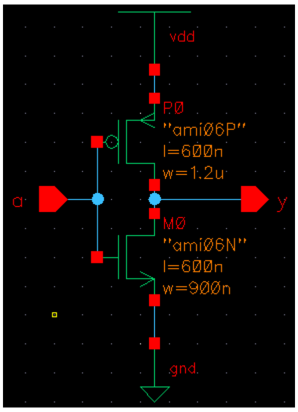
Effect of Anti Reflective coating



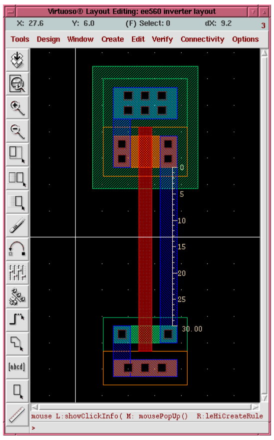
Impact generation rate in an Avalanche PhotoDiode

Introduction

CADENCE : Schematic and layout views



Schematic



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Layout

Light to silicon interaction

Class Level 1 : Light to silicon interaction

Light to silicon interaction

Incident Photons can be divided into two groups based on their energy compared to that of the silicon band gap (E_G =1.12eV) :

1. $E_{ph} < E_G$ Photons interact only weakly with the silicon, passing through it as if it were transparent.
2. $E_{ph} \geq E_G$ Photons are efficiently absorbed and each photon create an electron hole pair (photoelectric effect)

Reminder $\lambda(nm) = \dfrac{1240}{E(eV)}$

(here we consider a range from [1.12 eV – 3.2 eV] => [380nm -1107nm])

Light to silicon interaction

Reflection at the interface:

$$R = \frac{\phi_R}{\phi_i} = \frac{(n_{Si}-1)^2}{(n_{Si}+1)^2}$$

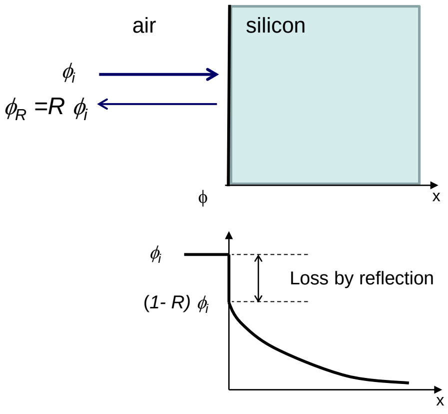
Photon flux at a x depth in silicon:

$$\phi(x,\lambda) = \phi_i(\lambda)(1-R)\, e^{-\alpha(\lambda)x}$$

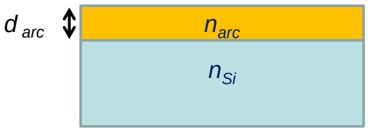
with $\alpha(\lambda)$: absorption coefficient

e/h Generation Rate in a thin silicon slice

$$G(x,\lambda) = \phi_i(\lambda)(1-R)\,\alpha(\lambda)e^{-\alpha(\lambda)x}$$



Passivation / Anti-reflection coating layers



Optimal refractive index of the anti-reflection coating: $n_{arc} = \sqrt{n_{air} n_{Si}}$

n_{Si}	~3,4
n_{Si3N4}	~2.05
n_{SiO2}	~1.54

Optimal thickness of the anti-reflection coating : $d_{arc} = \dfrac{\lambda}{4n_{arc}}$

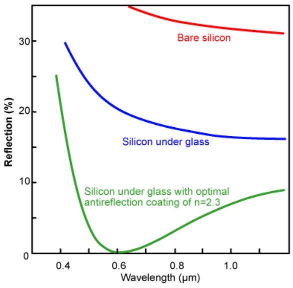
Passivation / Anti-reflection coating layers

Reflectance at normal incidence

$$R = \frac{r_1^2 + r_2^2 + 2r_1\, r_2\, \cos 2\theta}{1 + r_1^2 r_2^2 + 2r_1\, r_2\, \cos 2\theta}$$

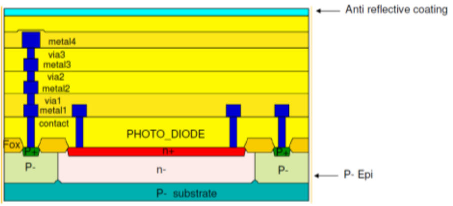
with:

$$r_1 = \frac{n_0 - n_{arc}}{n_0 + n_{arc}} \qquad r_2 = \frac{n_{arc} - n_{Si}}{n_{arc} + n_{Si}} \qquad \theta = \frac{2\pi n_{arc} d_{arc}}{\lambda}$$

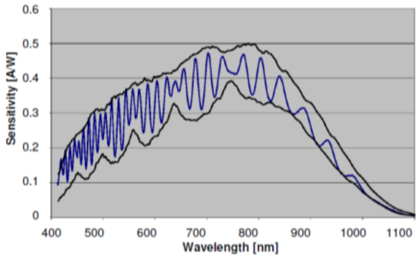


Passivation / Anti-reflection coating layers

Example: AustriaMicroSystems CMOS-Opto 0.35µm technology



C35-Opto Process Cross-Section



® AustriaMicroSystems

Class Level 1 : Simulations

1) **Absorption depth**

- Evaluate the absorption depths at λ = 400nm, 600nm, 900nm defined as the depth into the material at which the photon flux drops by a factor of 1/e (~36%).

- Evaluate the absorption coefficient for 400nm, 600nm, 900nm and look for a relationship between absorption depth and absorption coefficient.

2) **Maximum generation rate**

- Evaluate the depths required to achieve the maximum generation rate at 400nm, 600nm et 900 nm.

3) **AR coating**

- Calculate the optimal refractive index of the AR coating for silicon ?
- Calculate the optimal thickness for a photodetection @ λ = 500nm ?
- Replace the coating by silicon nitride (Si3N4) and silicon oxide (SiO2), redo the layer thickness optimization @ 500 nm for these materials.

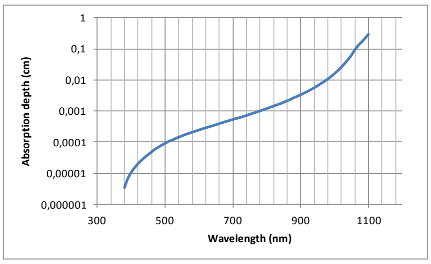
Class Level 1 : Reminder

1) **Absorption depth – Generation rate**

The absorption depth is simply the inverse of the absorption coefficient

A shallow junction will be more sensitive to in the near UV-Blue range

Deeper junction will be more sensitive in the red-near IR range



2) **Passivation layer and AR coating**

These layers have a significant impact on the photodiode response (modulation of the transmitted flux)

CMOS Photodiodes

Class Level 2 CMOS Photodiodes

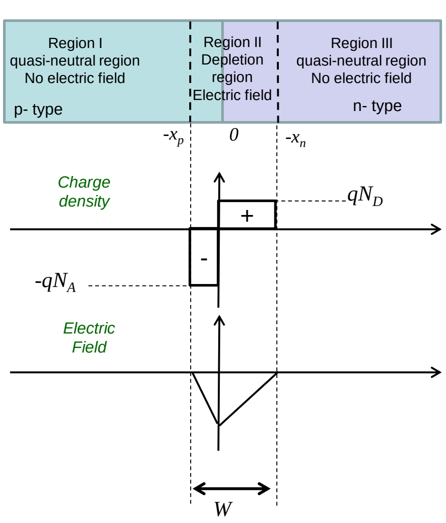
Space-charge or depletion region

Build-in voltage (Barrier height):

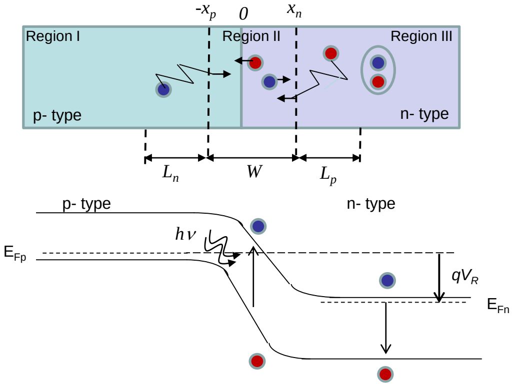
$$V_0 = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right)$$

Total Depletion Width under reverse biasing:

$$W = x_p + x_n = \sqrt{\frac{2\varepsilon}{q}(V_0 + V_R)\left(\frac{1}{N_A} + \frac{1}{N_D}\right)}$$



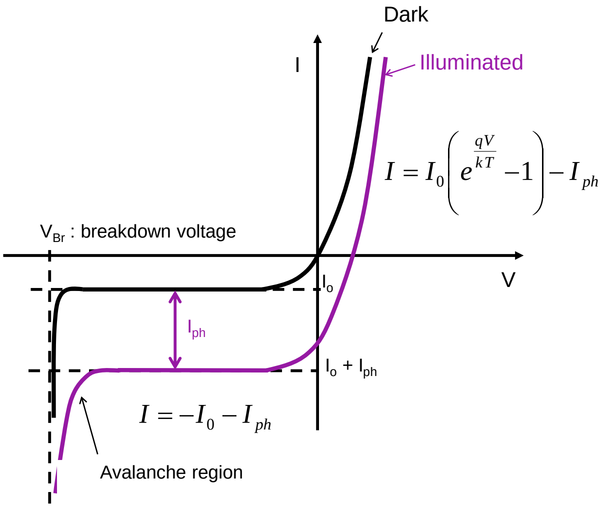
Photocurrent



The photocurrent has two components (reverse biasing):

$$I_{ph}(\lambda) = \underbrace{\boxed{qA\int_{-x_p}^{-x_p-L_n} G(x,\lambda)dx + qA\int_{x_n}^{x_n+L_p} G(x,\lambda)dx}}_{\text{Diffusion}} + \underbrace{\boxed{qA\int_{-x_p}^{x_n} G(x,\lambda)dx}}_{\text{Drift}}$$

Photocurrent



$$I = I_0\left(e^{\frac{qV}{kT}} - 1\right) - I_{ph}$$

$$I = -I_0 - I_{ph}$$

$$I_0 = qAn_i^{\,2}\left\{\frac{D_n}{N_A L_n} + \frac{D_p}{N_D L_p}\right\}$$

Planar diffused silicon photodiode

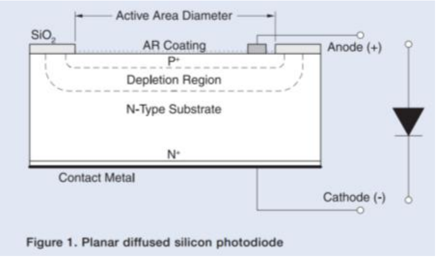
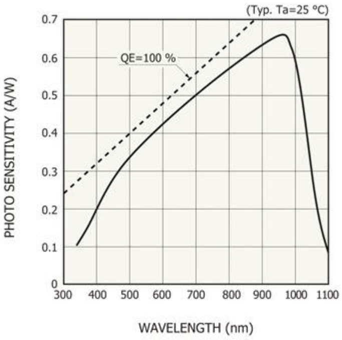


Figure 1. Planar diffused silicon photodiode



Class Level 2 : Simulations

1) **Impact of the reverse biasing**

- Calculate the built-in voltage for the default doping values @ 300K
- Evaluate the drift current contributions for reverse biasing voltage of 0V, -2V, -5V, -10V?
- Evaluate the spectral response changes for these reverse biasing voltages

2) **Passivation layer / AR coating**

- implement your optimized AR coating, and the Si3N4 and SiO2 passivation layers
- Compare the obtained spectral response with those achieve with CMOS AMS 0.35µm technology

3) **Evaluation of other parameters influence such as Temperature, Doping concentrations, …**

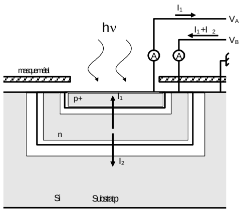
Class Level 2 : Reminder

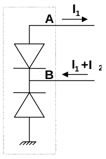
1) Higher reverse biasing increases the drift component of the photocurrent (wider depletion region) but also increases the dark current.

2) Junction depth is a key parameter for the spectral response of the designed photodiode

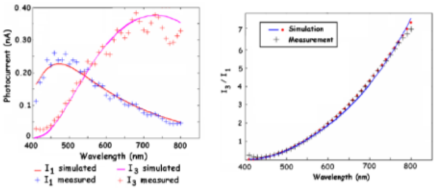
3) Photodiode design is strongly related to the CMOS technology parameters. Several types of photodiodes can be designed within a given process.

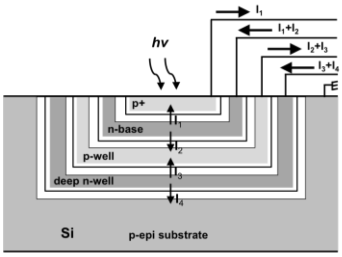
Multi buried junction photodetectors



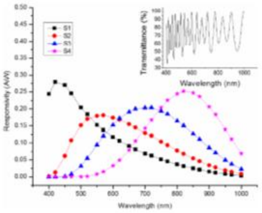


Buried Double junction photodetectors
(BDJ)





Buried Quad junction photodetector
(BQJ)



Class Level 3 : Simulations

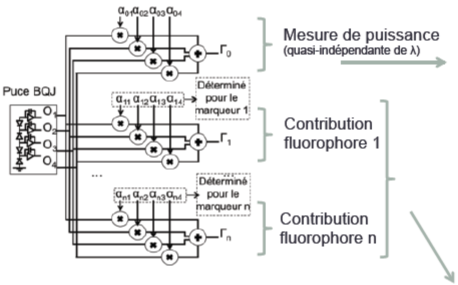
-1) **photo current ratio**

- modify the incident photon flux and observe the impact on the photocurrent ratio : any explanation ?
- modify the ARC coating properties and observe the evolution of the photocurrent ratio : any explanation ?
- measure the wavelengths corresponding to photocurrent ratios of 0.2 and 5.0: Evaluate these wavelength with an error of 10% on each current ; Conclusions

-2) **Photocurrent weighting**

- how could you qualify the BDJ photodetector output “I_1+I_2” in term of spectral response and efficiency as compared with individual photodiodes outputs ?
- Could you find a better weighting of the BDJ output in terms of the flatness of the response

Class Level 3 : Simulations

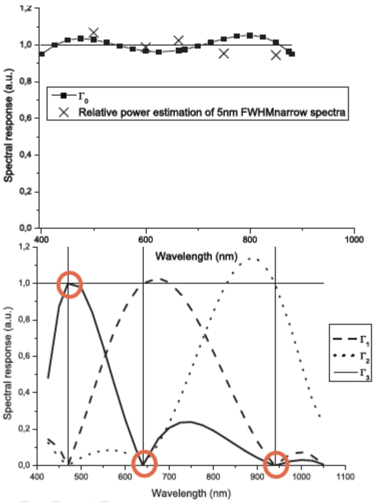


Mesure de puissance
(quasi-indépendante de λ)

Contribution fluorophore 1

Contribution fluorophore n

$$\begin{bmatrix}\Gamma_0\\ \Gamma_1\\ \dots\\ \Gamma_n\end{bmatrix}=\begin{bmatrix}\alpha_{01} & \alpha_{02} & \alpha_{03} & \alpha_{04}\\ \alpha_{11} & \alpha_{12} & \alpha_{13} & \alpha_{14}\\ \dots & \dots & \dots & \dots\\ \alpha_{n1} & \alpha_{n2} & \alpha_{n3} & \alpha_{n4}\end{bmatrix}\begin{bmatrix}I_1\\ I_2\\ I_3\\ I_4\end{bmatrix}$$

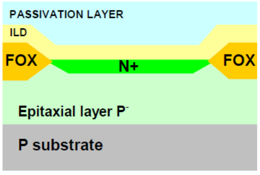


Γ_1, Γ_2 et Γ_3, pour
λ1=470nm, λ2=640nm et λ3=940nm

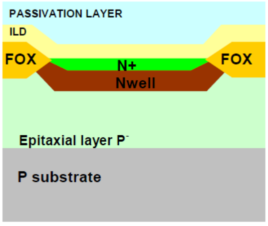
Complements

Photodiode implementation in AMS CMOS-Opto 0.35µm technology

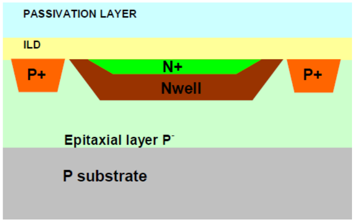
ILD: Interlevel Dielectric oxide
FOX: Field Oxide



photodiode 1



photodiode 2

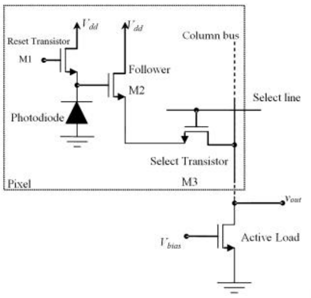


photodiode 3

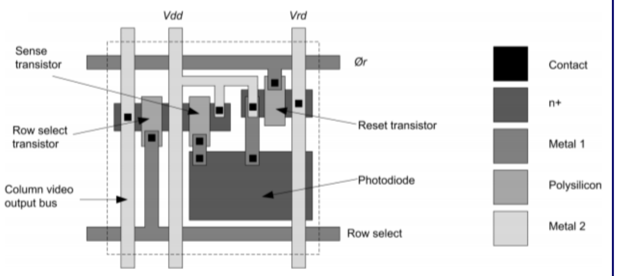
	photodiode 1	photodiode 2	photodiode 3
Quantum efficiency (Peak)	29%	43%	43%
Dark current (nA/cm²) @20°C	1.0	0.4	4.3

P. Martin-Gonthier et al. Proc. SPIE 5978, 2005

Conventional 3T CMOS Active Pixel Sensor : Architecture and Layout

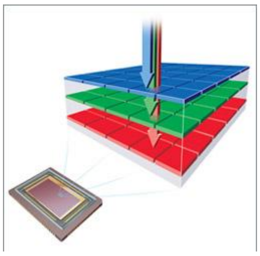


- Optimization of the fill factor / resolution tradeoff
- Charge amplification through the junction capacitance



® *Nick Waltham*
Rutherford Appleton Laboratory

Multi buried junction photodetectors: commercial implementation

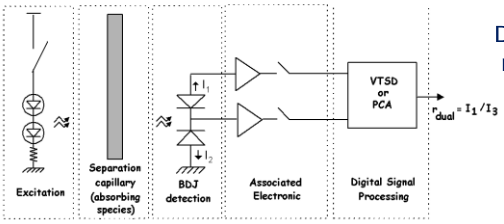


46 megapixel 24×16mm APS-C X3 Full-color image sensor

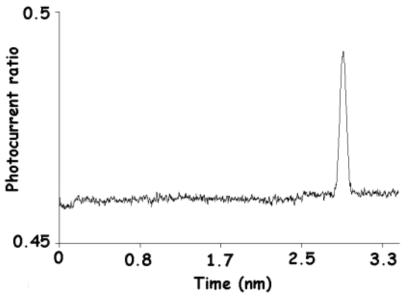
A Dramatically Different Design

The revolutionary design of Foveon X3 direct image sensors features three layers of pixels. The layers are embedded in silicon to take advantage of the fact that red, green, and blue light penetrate silicon to different depths — forming the world's first direct image sensor.

Multi buried junction photodetectors: example of signal processing



Dual-wavelength absorptiometry method for BDJ photodetection



Robust and compact alternative method to conventional differential methods
(only one optical path is required)

Conclusion and debriefing