l Summer School on INtelligent Signal Processi

Abstracts book

Table of contents

Abstract ID : 52

LAB8 - MicroTCA at CMS (Francesco Costanza)

Content :

After nearly three decades and more than two generations of HEP experiments VME is on the way to be replaced as the technology used all over the place. Having the good experiences with using industry standards in mind the different flavours of PICMG's TCA (Telecommunications Computing Architecture) seem to be the winner. At CMS we focussed on MicroTCA MTCA.0. While providing well-defined standards for crates, power supplies, housing of readout cards the backplane of a uTCA crate is able to cope with the data transport requirements of the current and next generation's HEP experiments. This was archieved by the quite common step from parallel to point-to-point serial data transfer (like USB, SATA, PCIe). Additionally the star topology of the uTCA connectivity fits well the main tasks of readout systems in HEP: collect the data of many readout units at a central place for further processing or storing.
In this exercise we would like to introduce another feature of uTCA which wasn't available before: a clocking network on the backplane which can be used to provide all boards with central clocking information. In our case it's the LHC clock: most of the readout units have to syncronize to this clock and a deterministic jitter behaviour is essential. With some simple tests we would like you to measure a few basic numbers on clock stability and jitter in our uTCA setup.

Primary authors : COSTANZA, Francesco (DESY)

Co-authors :

Presenter : COSTANZA, Francesco (DESY)

Track classification :

Contribution type : --not specified--

Submitted by : GALLO, Elisabetta

Submitted on Friday 31 July 2015

Last modified on : Friday 21 August 2015

Comments :

Abstract ID : 53

CLAB2 - "Parametric Study of CMOS Photodetectors" (Patrick Pittet, Francis Calmon, Rémy Cellier, Laurent Quiquerez, CNRS-INL, FR)

Content :
Some key design parameters for silicon photodiodes and CMOS multi-buried junction photodetectors are first introduced and then studied with a Matlab simulation tool. The computer aided class is organized in three sections: Section 1 deals with wavelength sensitive light to silicon interactions (passivation layer reflections, absorption, electron/hole generation rate, ...). Section 2 covers a parametric study of CMOS photodiode design (junction depth, junction biasing, doping concentration, oxide layer thickness, ...). Section 3 gives a special focus on CMOS multi-buried junction photodetectors, which consists of vertically stacked photodiodes.

Primary authors : CALMON, Francis (Lyon)

Co-authors :

Presenter : CALMON, Francis (Lyon)

Track classification :

Contribution type : --not specified--

Submitted by : GALLO, Elisabetta

Submitted on Friday 31 July 2015

Last modified on : Friday 21 August 2015

Comments :

Abstract ID : 54

LAB1 - "Hands on Pixel Front End ASICs" Lodovico Ratti (Pavia U. and INFN, IT) and Valerio Re (Bergamo U., IT)

Content :

The focus of the lab will be the experimental characterization of a front-end channel for pixel detectors in a 65 nm CMOS technology. Pixel Front-End ASICs are located at the very beginning of the Signal Processing chain in pixel-based detectors used in many fundamental and applied research fields. So, generally speaking, testing of front-end circuits in advanced microelectronic technologies is an integral part of the implementation of modern radiation detection systems.
During the laboratory session, after a short introduction on the device under test and the test set up, students will learn how to use basic electronic instrumentation (a power supply, a digital scope, a waveform/arbitrary function generator) to configure the circuit and measure the main electrical parameters.
While no previous experience in pixel front-end characterization is required, basic knowledge on electronic circuit operation and standard bench top instrumentation is a prerequisite.

Primary authors : RE, Valerio (Bergamo)

Co-authors :

Presenter : RE, Valerio (Bergamo)

Track classification :

Contribution type : --not specified--

Submitted by : GALLO, Elisabetta

Submitted on Friday 31 July 2015

Last modified on : Friday 21 August 2015

Comments :

Abstract ID : 56

LAB3: TARGET, Front End Electronic module for the Gamma-ray Cherenkov Telescope for CTA (Garrett Cotter, Oxford)

Content :

The Gamma-ray Cherenkov Telescope (GCT) is proposed to be part of the Small Size Telescope (SST) array of CTA (the Cherenkov Telescope Array). The GCT camera is designed to record the flashes of Cherenkov light from gamma-ray initiated electromagnetic cascades, which last only a few tens of nanoseconds. Modules based on “TARGET” ASICs provide the required fast electronics, allowing sampling at 1 GSample/s and digitization, as well as first level of triggering using the analogue outputs of the photosensors. In this lab we give an overview of the challenges casted by the technique to observe high energy gamma ray with ground based telescope and we present TARGET, the Front End Electronics module used in the GCT camera. During the lab session the student will be provided with all the necessary lab kit to reproduce a miniature version of the telescope effectively recording light mimicking the Cherenkov light emission from electromagnetic air shower.

Primary authors : COTTER, Garrett (Oxford)

Co-authors :

Presenter : COTTER, Garrett (Oxford)

Track classification :

Contribution type : --not specified--

Submitted by : GALLO, Elisabetta

Submitted on Thursday 13 August 2015

Last modified on : Friday 21 August 2015

Comments :

Abstract ID : 58

CLAB6: Multi/Many-Core programming with Intel Xeon Phi Coprocessors - Fundamentals of Parallel Programming using Intel's Many Integrated Core (MIC) Architecture (R. Iope, S. Stanzani, R. Cobe, SPRACE, UNESP, BR)

Content :

The Intel Xeon Phi coprocessor, the first product of Intel's Many Integrated Core (MIC) Architecture, is an accelerator technology developed by Intel to enable performance gains for highly parallel computing workloads with interesting and appealing features, including the ability to use familiar programming models such as OpenMP and MPI. This hands-on training session is a comprehensive, practical introduction to parallel programming based on the Xeon Phi architecture and programming models, aiming to demonstrate the processing power of the Intel Xeon Phi product family.

Attendants of CLAB2 & CLAB3 will start issuing simple command-line tools to get basic information about the Intel Xeon Phi coprocessors, then learn how to monitor what resources are being used and access their operating systems by establishing ssh sessions with them. They will thus verify that the Intel Xeon Phi coprocessor is an IP-addressable PCIe device - managed by an independent environment provided by the MIC Platform Software Stack (MPSS) - that runs a Linux-based operating system.

Following the introductory part, participants will learn how to compile and run simple C/C++ applications directly into the coprocessors, and then compile and run example codes based on shared-memory parallelism with OpenMP and Cilk Plus and distributed-memory parallelism with MPI. They will also work on MPI application examples that should be executed simultaneously on the Xeon processors and the Xeon Phi coprocessors, explore the use of Intel libraries TBB and MKL, and develop insights on tuning parallel applications.

Summary :

Proposed Agenda:

Participants of CLAB2 and CLAB3 will work on predefined sets of exercises that progressively help them get familiar with the Intel Xeon Phi coprocessor hardware, programming models and development tools. Exercises have been developed in such a way that the learners proceed from one topic to the next at their own speed.

CLAB2: Exploring the Intel Xeon Phi coprocessor architecture
The first lab session will start with an introductory lecture providing a concise overview about the Xeon Phi coprocessor and a live demonstration on how to access the remote system. The practical activities will then allow participants to apply the learned concepts with lab exercises using the Intel Xeon Phi coprocessors installed on the server.

Topics:
- Introduction to Parallel Programming
- Overview of the Intel Xeon Phi hardware architecture
- Overview of the Intel Xeon Phi programming environment
- Compiling and running trivially simple applications
- High performance test-drive

CLAB3: Exploring the Intel Xeon Phi application development tools
The second lab session builds on information learned during the first session, providing extra coverage with exercises that highlight task parallelism using OpenMP and Cilk Plus, stress MPI specific key concepts, and develop some optimization strategies. The session concludes with an exercise that shows how to improve the performance efficiency of applications developed for the Xeon Phi.

Topics:
- Data parallelism: Fundamentals of vectorization
- Task parallelism: OpenMP and Cilk Plus
- Process parallelism: MPI programming models and hybrid OpenMP/MPI
- Optimization strategies for MPI applications
- Application performance tuning: optimizing a real-world code example

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Track classification :

Contribution type : --not specified--

Submitted by : GALLO, Elisabetta

Submitted on Tuesday 18 August 2015

Last modified on : Friday 21 August 2015

Comments :

Abstract ID : 60

LAB2: Transient Current Technique (TCT) measurements for Silicon Diodes (Christian Scharf and Erika Garutti, UniHH)

Content :

This experiment is meant to illustrate the signal formation in silicon-based radiation detectors and the effect of a read-out circuit on fast signals. Hands-on measurements are compared to simulations in order to see the effect of the read-out circuit on the signal. The transfer function of the read-out circuit is determined to disentangle read-out effects and the initial signal.

Primary authors : SCHARF, Christian (DESY)

Co-authors :

Presenter : SCHARF, Christian (DESY)

Track classification :

Contribution type : --not specified--

Submitted by : GALLO, Elisabetta

Submitted on Monday 31 August 2015

Last modified on : Monday 31 August 2015

Comments :

Abstract ID : 63

CLAB5: MPI for Parallel Computing by U. Marconi (INFN-Bologna), A. Falabella and M. Manzali (CNAF-INFN)

Content :

The end of the exponential growth in single-processor performance marks the end of the dominance of the single microprocessor in computing,
giving way to a new era, in which computer parallelism is at the forefront.
MPI (Message Passing Interface) is a communications protocol used for programming parallel computers.
It has become a standard for communication among processes that model a parallel program running on a distributed memory system.
The laboratory lectures consists of two parts.
The first part will present MPI concepts and functionalities.
The hands-on session will provide a set of MPI programming exercises, which will help to understand the basic ideas of MPI
parallel programming by demonstrating the key features of message passing interface through the sample programs.

Primary authors : MARCONI, Umberto (INFN Bologna)

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Track classification :

Contribution type : --not specified--

Submitted by : GALLO, Elisabetta

Submitted on Wednesday 09 September 2015

Last modified on : Thursday 10 September 2015

Comments :

Abstract ID : 64

Lab6&7: Field Programmable gate arrays – Detecting Cosmic Rays by D. Cussans (Bristol U. UK)

Content :

Field-Programmable-Gate-Arrays (FPGAs) play an increasingly important role in instrumentation for particle physics. In this exercise students will develop firmware to read-out a simple scintillation detectors and hence detect cosmic-ray-muons

Summary :

A Xilinx FPGA evaluation board is coupled to discriminators attached to photo-multiplier-tubes instrumenting plastic scintillator.

Students will engage in one of more of the following activities

1) Write HDL code to fit into an existing VHDL framework. This code will do one or more of the following functions: Count pulses,Time-stamp pulses, Detect coincidences. These data will be read-out to a PC over Ethernet using a firmware module supplied.
2) Operate and modify a test-bench to allow simulation and verification of the design.
3) Write or modify a Python script to read and analyse the data.
4) Any other (sensible) activity.

The Xilinx ISE environment will be used for HDL synthesis and either ModelSim or ISIM for simulation.

Estimated Time for Completion
For a student that has not encountered HDL synthesis for FPGAs and/or the use of Python as a scripting language it is anticipated that to complete all the activities will take approximately 4-5 hours. Hence the lab is advertised as two sessions. Students can do either one or both sessions.

Primary authors : CUSSANS, David (Bristol)

Co-authors :

Presenter : CUSSANS, David (Bristol)

Track classification :

Contribution type : --not specified--

Submitted by : GALLO, Elisabetta

Submitted on Thursday 10 September 2015

Last modified on : Thursday 10 September 2015

Comments :