Vertical Integration in New Devices

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Abstract

I will discuss the techniques and challenges associated with the vertical integration of integrated circuits currently used in modern experiments and also under development for future applications. I will (try to) cover some of the technologies used for bump bonding, some of the challenges encountered in recent applications, followed by the motivation for and experience with direct vertical wafer interconnects. Examples will be the PSI46 (new version of the Front End ASIC for the Pixel vertex detector in CMS) and FE-I4b (the Front End ASIC for the intermediate layer IBL included now in ATLAS innermost tracking system), two Read Out Chips bump bonded to pixel sensors and experience with the direct bonded VIPIC (Vertically Integrated Photon Imaging Chip) chip and experience with vertical interconnects in the VIPRAM (Vertically Integrated Pattern Recognition Associative Memory) project.