Kintex Ultrascale based MTCA digitizer cards, the SIS8300-KU and beyond
SIS8300-KU
10 channel 125 MSPS 16-bit digitizer
(250 MSPS 14-bit stuffing option)

History

Virtex 5 based
2010 SIS8300 initial development, first MTCA.4 board
2011 SIS8300 V2 > 340 units in field (in part 8 channel 250 MSPS 14-bit BPM)

Virtex 6 based
2014 SIS8300-L > 150 units in field
2015 SIS8300-L2x > 750 units in field (L2S, L2D, …)
First of all thanks to:

Lund University  
For driving the development with the initial 5 unit order and a development cost contribution

DESY  
For continued support with the SIS8300-x developments. In particular KU power supply development considerations and upcoming SIS8300-KU/DWC8300 LLRF qualification (amplitude and phase noise, time jitter and amplitude stability)

Andreas Grüttner  
For yet another ready to ship Rev. 1 schematic and layout
One of the first 10 SIS8300-KU's
SIS8300-KU versus L2 changes

- New Power Supply Scheme
- RJ45 I/O instead of Harlink
- SFP+ instead of SFP
- DDR4 memory instead of DDR3
- PCIe Gen3 instead of Gen1/2
- Kintex Ultrascale instead of Virtex 6
- WR Option
SIS8300 Properties
(refer to flyer in conference bag also)

- 10 Channels 125 MS/s 16-bit ADC
- 10 MS/s to 125 MS/s Per Channel Sampling Speed
- AC or DC Input Stage
- Internal, Front Panel, RTM and Backplane Clock Sources
- Two 16-bit 250 MS/s DACs for Fast Feedback Implementation
- High Precision Clock Distribution Circuitry
- Programmable Delay of Dual Channel Digitizer Groups
- Multi Gigabit Link Port Implementation to Backplane
- Twin SFP+ Card Cage for High Speed System Interconnects
- White Rabbit Clock Option for SFP+ Ports
- Two RJ45 Connectors (One Clock + 3 Data or 4 Data In/Out)
- XCKU040-1FFVA1156C Kintex Ultrascale FPGA
- 2 GByte DDR4 Memory (flexible partitioning scheme)
- 4 lane PCI Express Gen3 Connectivity
- Dual boot
- MMC1.0 under DESY license LV91
- In Field Firmware Upgrade Support
- Zone 3 class A1.0, A1.0C or A1.1CO Compatible
Technical Aspect I: PCB Layer Stack

Megtron 6 layers because of Gen3 PCIe and SFP+ speeds

Maintain FR4 on outer layers for "hand" configuration soldering

Note: like all SIS8300-x PCBs produced by Heger in Norderstedt
Technical Aspect II: Backdrilled Vias

Decreasing via stub length by backdrilling significantly reduces a particularly problematic form of signal distortion called deterministic jitter. Because Bit Error Rate (BER) is strongly dependent on deterministic jitter, any reduction in deterministic jitter by backdrilling will significantly reduce the overall BER of the interconnect – often by many orders of magnitude. Other key advantages to backdrilling PTH vias include less signal attenuation due to improved impedance matching, increased channel bandwidth, reduced EMI/EMC radiation from the stub end, reduced excitation of resonance modes and reduced via-to-via crosstalk.

48 backdrilled vias for 4 PCIe lanes and SFP+ MGTs

Drawing source: www.multi-circuit-boards.eu
Text source: www.sanmina.com
SIS8300-KU White Rabbit (WR) Ready

- PLL Clock Synthesizer
- VCO, VCXO
- DACs for VCO Control
- Additional Power

No known Kintex UltraScale White Rabbit PTP Core (WRPC) yet

What is WR?
Sub ns synchronisation
Synchronous Ethernet
IEEE 1588 PTP
# FPGA Resources/Performance

<table>
<thead>
<tr>
<th>Used FPGA</th>
<th>XC6VLX130T-2FFG1156C (SIS8300-L2)</th>
<th>XCKU040-1FFVA1156C (SIS8300-KU)</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Logic Cells</td>
<td>128 K</td>
<td>500 K</td>
</tr>
<tr>
<td>CLB LUTS/Flip-Flops</td>
<td>80/160 K</td>
<td>242/484 K</td>
</tr>
<tr>
<td>Block RAM/FIFO w/ECC (36Kb each)</td>
<td>264</td>
<td>600</td>
</tr>
<tr>
<td>Block RAM/FIFO (18Kb each)</td>
<td>528</td>
<td>1200</td>
</tr>
<tr>
<td>Total Block RAM (Mb)</td>
<td>9.5</td>
<td>21.1</td>
</tr>
<tr>
<td>DSP Slices</td>
<td>480</td>
<td>1920</td>
</tr>
<tr>
<td>GTH speed</td>
<td>6.6 Gb/s</td>
<td>16.3 Gb/s</td>
</tr>
<tr>
<td>PCIe</td>
<td>Gen2</td>
<td>Gen3</td>
</tr>
<tr>
<td>Memory Controller</td>
<td>DDR3</td>
<td>DDR4</td>
</tr>
</tbody>
</table>
SIS8300-KU to SIS8300-L2
Payload Power Consumption Comparison
Comparable Firmware Design
(currently more memory/diagnostics in KU)

<table>
<thead>
<tr>
<th>Board Type Firmware Design</th>
<th>SIS8300-L2 8302100F</th>
<th>SIS8300-KU 83039905 (prelim)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Up</td>
<td>2,9 A</td>
<td>2,6 A</td>
</tr>
<tr>
<td>P2P and FP Link Test</td>
<td>3,1 A (1Gbit/s)</td>
<td>2,8 A (10Gbit/s)</td>
</tr>
<tr>
<td>Memory Test</td>
<td>3,2 A</td>
<td>2,8 A</td>
</tr>
<tr>
<td>ADC „ROOT“ Test</td>
<td>3,5 A</td>
<td>3,2 A</td>
</tr>
</tbody>
</table>

Conclusion:
About 10% lower at (partially) substantially higher performance
SIS8300-x ROOT GUI
SIS8300-KU 8AC2DC with SIS8900 RTM

RMS for open AC/DC channel
10 Unit Prototype series (all 8AC2DC DZ3 configuration) out of stuffing mid November 2016, **all in working order**

- First Lund University and ESS/ERIC shipments next week
- One unit for DESY reference/cross L2 measurements
- One reference unit at Struck

Production of initial 20 unit production batch under way

- Xilinx FPGAs confirmed for next week
- PCBs confirmed for week 3 of 2017
- Availability of cards mid February 2017
JEDEC Solid State Technology Association, formerly known as the Joint Electron Device Engineering Council (JEDEC) Independent semiconductor engineering trade organization and standardization body

- **2006** JESD204 multigigabit serial data link between converter(s) and a receiver
- **2008** JESD204A multiple aligned serial lanes, lane speed up to 3.125 Gbps
- **2011** JESD204B provisions to achieve deterministic latency, lane speed up to 12.5 Gbps
- **Future** JESD204C, Line rates from 1 Gb/s to 32 Gb/s and 64B/66B encoding
JESD204B Advantages I
→ basis for many new digitizer chips

Layout/Routing

Classic: 18 differential LVDS signal pairs per dual 125 MSPS 16-bit ADC

JESD: one or two pairs/lanes plus sync.
JESD204B Advantages II

→ basis for many new digitizer chips

- Lower power at higher speeds
- Constant power draw
- No multiple synchronous bit flips
- Serial data stream rather than data to strobe at the right point in time (FPGA tap delay)

Recommended Reading

Analog Devices: JESD204B Survival Guide
### Some High Speed JESD204B Digitizer Chips

<table>
<thead>
<tr>
<th>Source</th>
<th>Chip</th>
<th>Sampling Speed MSPS</th>
<th>Bits</th>
<th>Chs</th>
<th>BW in MHz</th>
<th>Lanes</th>
<th>PWR per Channel in W</th>
</tr>
</thead>
<tbody>
<tr>
<td>TI</td>
<td>ADS54J54</td>
<td>500</td>
<td>14</td>
<td>4</td>
<td>900</td>
<td>8</td>
<td>0.9</td>
</tr>
<tr>
<td>TI</td>
<td>ADS54J60</td>
<td>1000</td>
<td>16</td>
<td>2</td>
<td>1200</td>
<td>4/8</td>
<td>1.4</td>
</tr>
<tr>
<td>ADI</td>
<td>AD9680</td>
<td>1000/1250</td>
<td>14</td>
<td>2</td>
<td>2000</td>
<td>4</td>
<td>1.7</td>
</tr>
<tr>
<td>ADI</td>
<td>unreleased</td>
<td>2500</td>
<td>14</td>
<td>2</td>
<td>5000</td>
<td>8</td>
<td>1.7</td>
</tr>
</tbody>
</table>

→ XCKU060-1FFVA1156C or “better” required for MGT availability reasons on higher channel count MTCA boards
ADI AD9680 Dual GSPS 14-bit Eval Kit (Avnet AES-KCU-JESD-G)

Data from ADI GUI read into TI GUI
ADI AD9680 Dual 1000 MSPS 14-bit

Data from ADI GUI read into TI GUI

ENOB $F_{in}$ 170 MHz 10.7 Bit

Evaluation Setup

- Limited to 580 MHz BW
TI ADS54J60 Dual GSPS 16-bit Eval Board (FMC+Intel Arria Carrier)

 Evaluation Setup
- Limited to 300 MHz BW
- Clock spurs

ENOB $F_{in}$ 170 MHz 11.3 Bit
Architecture Example ADS54J60 (multiple cores)
ADI unreleased Dual 2.5 GSPS 14-bit

Architecture equivalent to AD9691
ADI unreleased Dual 2.5 GSPS 14-bit Eval Board („FMC“+Xilinx Virtex 7 Carrier)

80 MHz sine
Axis scaled to 16-bit

Prelim user manual: $f_{\text{IN}} = 170$ MHz, ENOB = 10.2 bits, analog bandwidth 5 GHz
Possible new MTCA Product
SIS8310 Quad 2.5 GSPS 14-bit Digitizer (Reduced Dual Channel Option)

Same carrier can be used for 8 channel 14/16-bit GSPS design FMC or custom tbd.
### MTCA.4 Relevance

**current Struck user base**

<table>
<thead>
<tr>
<th>Country</th>
<th>Institution</th>
</tr>
</thead>
<tbody>
<tr>
<td>AU</td>
<td>Australian Synchrotron*</td>
</tr>
<tr>
<td>BR</td>
<td>LNLS*</td>
</tr>
<tr>
<td>CN</td>
<td>IHEP Beijing, SINAP</td>
</tr>
<tr>
<td>CZ</td>
<td>ELI (Inst of Physics, Praha)</td>
</tr>
<tr>
<td>DE</td>
<td>DESY, HZDR, PTB, MPG, KIT, HZB, GSI, DESY Zeuthen</td>
</tr>
<tr>
<td>ES</td>
<td>ESS Bilbao*</td>
</tr>
<tr>
<td>FR</td>
<td>ITER, Saclay*</td>
</tr>
<tr>
<td>IN</td>
<td>TIFR</td>
</tr>
<tr>
<td>JP</td>
<td>KEK, SPring-8</td>
</tr>
<tr>
<td>KR</td>
<td>PAL</td>
</tr>
<tr>
<td>RU</td>
<td>ITER</td>
</tr>
<tr>
<td>SE</td>
<td>ESS, Lund University</td>
</tr>
<tr>
<td>US</td>
<td>SLAC, NSCL/FRIB, ANL</td>
</tr>
</tbody>
</table>

expected to join shortly: TR TARLA, US ORNL

* new in 2016
Questions/Discussion
Backup: DDC Block of AD9691