Implementation of GigE Vision Standard and Applications in MicroTCA

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AGENDA

1. GigE Vision Camera Support – Why?
2. FPGA IP-Core Advantages
3. System Realization
4. GigE Vision Implementation
5. Application Concepts
Why GigE Vision Camera Support?

- Integrate into existing control system
- Outsource image processing to FPGA
- Algorithms can run in parallel
- Flexibility is same as in software

- Simple cabling (up to 100 m, PoE)
- Faster transfer rate than Firewire
- ROI definition is possible
- Device precision time protocol (IEEE1588)
FPGA IP- Core Advantages

Target product:

- Firmware that is modular, scalable and widely usable
- IP-Core for Vivado Design Suite integration
- AXI4 / AXI-Stream compliant

- Basically MTCA independent
- Xilinx 7Series, Ultrascale, Ultrascale+, SoC and MPSoC compliant
- Licensing as official GigE Vision product by AIA is ongoing
System Realization

Firmware Development
- GigE Vision IP-Core
- TCK7 BSP

Software Development
- System controller
- Python and C++

https://github.com/MicroTCA-Tech-Lab
GigE Vision Firmware

- Software Interface via PCIe
- Send/Receive GVCP packets
- Receive GVSP packets
- Parse to AXI Video Stream
GigE Vision Firmware

Resource utilization GigE Vision IP-Core

<table>
<thead>
<tr>
<th>Primitive Type</th>
<th>Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>FLOP_LATCH</td>
<td>1114</td>
</tr>
<tr>
<td>LUT</td>
<td>1543</td>
</tr>
<tr>
<td>CARRY</td>
<td>184</td>
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<tr>
<td>BMEM</td>
<td>10</td>
</tr>
</tbody>
</table>

Performance GigE Vision Implementation

<table>
<thead>
<tr>
<th>Resolution</th>
<th>Frame Size</th>
<th>Framerate FPGA</th>
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</thead>
<tbody>
<tr>
<td>1920 x 1080 px</td>
<td>16.59 Mbit</td>
<td>50 fps</td>
</tr>
<tr>
<td>1936 x 1216 px</td>
<td>18.83 Mbit</td>
<td>48 fps</td>
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</tbody>
</table>

- Optimization is ongoing
- Test with faster cameras
- 10Gb Ethernet
GigE Vision Software

- Modular controller concept
- PCIe driver provided by Xilinx with DMA IP-Core
- Usable with OpenCV image processing library
- Support for Python and C/C++
Application Concepts

- Application code is written in C++
- Low latency (dimension dependent)
- Convenient debugging and analysis tools
Application Concepts

DAMC-FMC2ZUP
- Xilinx Ultrascale+ MPSoC
- ARM Mali GPU

DFMC-SFP4
- 4x SFP/SFP+

- Hardware and software on single chip
- Standalone solution

GigE Vision IP-Core and logic infrastructure

Controller Software

Image Data Processing

Processing System

Memory
DDR4/64L, LPDDR4X 32/64 bit w/eCC
256KB OCM with ECC

Graphics Processing Unit
ARM Mali™-400 MP2
Geometry Processor
Pixel Processor 1 2
Memory Management Unit
64KB L2 Cache

Platform Management Unit
System Management
Power Management
Functional Safety

Configuration and Security Unit
Config AES, Decryption, Authentication, Secure Boot
Voltage/Temp Monitor
TrustZone

System Functions
Timers, WDT, Resets, Clocking & Debug

High-Speed Connectivity
DisplayPort v1.2e
USB 3.0
SATA 3.1
PCIe® 3.0/2.0
PS-CTM

General Connectivity
GigE
USB 2.0
CAN
UART
SPI
Quad SPI NOR
NAND
SD/mMMC

Hardware and software on single chip
Standalone solution

from xilinx.com
Conclusion and Outlook

Products:

• GigE Vision IP-Core and infrastructure for DAMC-TCK7 (support for 8 cameras with single board)

• Standalone FPGA firmware solutions (UDP IP-Core, HLS processing application)

Ongoing projects:

• Image processing for PETRA-III Beamlines

• Porting for NAMC-ZYNQ-FMC with N.A.T.

• Firmware and software optimization