Electromagnetic Compatibility (EMC) in Modern Electronic Standards e.g. MicroTCA.4

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Hamburg, 04.12.2019
1 Why is EMC important for us?

- Example: Laser-RF-Locking, **not** optimized phase noise spectrum

A distortion free spectrum is a condition to achieve good time resolutions. Most of the distortions are self-made and can be fixed but some are related to EMC.

Do these distortion lines degrade the time resolution?

\[
\Delta t_{f_1,f_2}^2 = \frac{1}{(2 \pi f_0)^2} \int_{f_1}^{f_2} S_\phi(f) df
\]
1 Analog meets Digital in Modular Systems

- Commercial ADCs:

![Commercial ADCs Image]

Performance maintained?

![Performance maintained Image]

Spurfree spectral ADC data!

![Spurfree spectral ADC data Image]
1 Low-Level-Radio-Frequency (LLRF) Control

High-frequency regulation – main noise sources:

- Reference (MO)
- Actuator (ACT)
- Vector Modulator
- Controller
- FPGA
- ADC
- DAC
- Klystron
- Amplifier
- Waveguides
- Field Detector (DWC)
- FB Loop
- S_{\phi,MO}(f)
- S_{\phi,ACT}(f)
- S_{\phi,DWC}(f)
- S_{\phi,RES}(f)

Example:

- fs Cavity field stability requirements:
  - Amplitude stability: <0.005% = 5E-5
  - Phase stability: <0.005 deg, <10fs @1.3GHz
  - Typical signal levels in receivers are about 1V:
  - Measurement resolution must be <1V*1E-5=10uV
  - All voltages caused by EMC must be smaller than 10uV!

Typical PCB ground resistances are about 1mOhm:
- Maximum return ripple current 10uV/1mOhm=10mA

- EMC system planning
- EMC system packaging
1 EMC Zones – System Robustness to External Distortion

- **Rack-Level**

- **Crate-Level** (Modular systems e.g. MicroTCA.4)

  - Analog frontend, ADC, DAC
  - AMC RTM
  - FPGA
  - Digital Transmission Class D1.x
  - AMC RTM
  - FPGA
  - ADC, DAC
  - Analog frontend
  - JESD

  **Challenge**

  - AMC RTM
  - Analog Transmission Class A1
  - ADC, DAC
  - Analog frontend
  - AMC RTM
  - FPGA
  - ADC, DAC
  - Analog frontend

  **Recommendation**

  - <0.5mΩ

  **Rack-Level**

  - 50µΩ
2 AMC / RTM Zone: IF Detection for Cavity Field Regulation

XFEL 48-channel LLRF station:

- Supporting modules
- MicroTCA.4

- MTCA.4 incl. complete suite: LLRF/Diag./Interlocks/HOM
- Challenges:
  - Total: 27 RF station / 800 cavities / >3000 RF signals
  - Stability requirements < 0.01% & 0.01 deg (<10fs)
2 Signal Conditioning and Digital Processing

- High frequency Down-Converter
  (DRTM-DWC10, under license)

- Multi-Channel fast ADC Digitizer
  (SIS8300L2)

- 10 channel field detection
- S-band (700MHz - 4.0GHz)
- Resolution, 0.003%, < 10fs

- 10 channel ADCs (125Msps, 16-Bits)
- FPGA (Virtex6) pre-processing partial cavity vectors
- Low latency links via MTCA-backplane

Frontend Mixers
10 Channels
Differential IF Signals
10 channel ADCs AC, DC coupled
Single-ended
RF Signals
FPGA, LLL, SFPs
Differential LVDS
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2 LLRF-Systems: Channel performance

- Spectral purity: (1DUT)

  System's Fingerprint

  - Spectral purity: System's Fingerprint
  - Spur removed on active and ground side (EMC)
  - Several years of group work!

  - Receiver narrow-band phase noise
    - < 0.002°, <4.2fs (1.3GHz)
    - < 0.004°, <9.2fs (1.3GHz)
2 AMC / FMC Zone: Coarse Bunch-Arrival Time Monitor

- **DFMC-DS500**
  - direct sampling digitizer
  - 12 bits, 0.5 - 1 GSP/s
  - ADC 2.7 GHz @ 3dB
  - SE → DIFF Amplifiers (4.8 GHz)

- Front panel has no direct connection to GND
- hexagon stand-off no direct connection between carrier GND and mezzanine GND
- RF connector GND is isolated from front panel

**Courtesy of J. Zink**

- f_s = 500 MHz, f_in = 125 MHz
- FFT: mean of 100 x 8000 samples
- f_s = 500 MHz, f_in = 1.3 GHz
- FFT: 8000 samples
Distortions current paths and its reduction:

- Modulate ADC-CLK section
- Couple into differential inputs
- Couple into single-ended sections
- ESD-Strip or single-ended connector
- Bypassed to Chassis
- ESD-Strip
3 Grounding configurations in MicroTCA.4

Properties of the Ground System in MicroTCA.4 for Z3 analog transmission:

- Return currents and signals share the same ground, all slots share one ground.
- Available shorts: Chassis-to-Ground (MicroTCA.4), Chassis-to-AMC, Chassis-RTM.
- No bypass structures for boards, the ground is unshielded.

Main distortions sources:

- AMC, RTM Loads
- Power Supply Module
4 Crate Ground Modelling

Distortion Rejection:

\[ DR_i = 20 \log \left( \frac{U_i(s)}{U_{DIS}(s)} \right) \]

\[ U_{DIS}(s) = \sum_{i=1}^{N} H_{DIS,i}(s)U_i(s) \]

\[ U_{GND}(s) = \sum_{i=1}^{N} H_{GND,i}(s)U_i(s) \]
5 EMC Optimization

Improved local AMC, RTM ripples (active side)
approx. 10...20dB

Reduction of power-supply ground-chassis distortions
approx. 10...20dB

Improved the ground by return current redistribution
approx. 10...20dB

Short ground-chassis distortions of the power supplies
approx. 10dB

Bypass AMC, RTM ground distortions into the chassis
approx. 10dB

Improved the receivers CMR (project specific)
approx. 10dB
5 EMC Optimization

- Reduction of source ground-chassis distortions of the power supplies

![Graph showing reduction of distortions](image1)

- Reduction of AMC return ripples, Improved local AMC, RTM filter chains

![Diagram of filter chains](image2)

- Reduction of AMC return ripples
- Decoupling of AMC modules +12V

- Reduction of
  - DC/DC chopper lines,
  - Distortions and noise

- LDO: LF noise reduction <1MHz
- RF-filter: RF noise reduction >1MHz for ADCs, ultra-low clock jitter etc.
5 Measuring Ground Distortions

- Measuring the Ground-Chassis Distortions

**DAMC-EMI Functions:**
- Ground-to-Chassis measurements
- Power supplies measurements
- Voltage ground prober
- Vibrations measurements
- Ground influences from RTMs
## System Partitioning / Packaging for < -80dB Stability

- **CAL**
- **FR-END**
- **ADC**
- **FPGA**

*Strongly coupled together, except EMC in the information band is fully under control.*

**JESD interface towards an isolated FPGA**

**Problem of commercial digitizers in standards without frontends**

### High Frequency Applications

<table>
<thead>
<tr>
<th>MicroTCA.4 Configuration</th>
<th>AMC: ADC ext.: FR-END</th>
<th>AMC or RTM: FR-END + ADC</th>
<th>AMC: ADC RTM: FR-END</th>
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<tbody>
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<td>Depend on EMC</td>
<td>Good, Excellent for optical inputs</td>
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<tr>
<td>-</td>
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### Baseband Applications

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<tbody>
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<td>Depend on EMC (strongly)</td>
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<td>Excellent</td>
</tr>
<tr>
<td>-</td>
<td>Very good</td>
<td>Very good</td>
<td>open - to be tested</td>
<td>Excellent</td>
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- Problem of commercial digitizers in standards without frontends

- **CAL**: adressed in this presentation
6 Future EMC Challenges: MicroTCA.4 digital Upgrades

- **MicroTCA.4 AMC Backplane Connections PCIe gen5:**
  - 10Gbase-KR Ethernet
  - Slim-pipe support ≥20Gbps NRZ per lane
  - Update fat pipes to support 32Gbps NRZ (and **56Gbps** PAM-4, 16GHz BW) per lane minimum (PCIe gen5, 200Gbase-KR4).

- **EMC related tasks:**
  - MTCA backplane connector crosstalk tests
  - Impact of moving MCH to the center to reduce channel length will be evaluated
  - Payload power per slot to 240W with better isolation
  - Ground-Chassis-Distortion to be improved by -20dB
  - Verification with next generation receivers
6 Future EMC Challenges: MicroTCA.4 Receiver Roadmap

- Improvement of Ground-Chassis Distortion by -20dB:

  **Receiver Improvements (<1fs, <100as, SRF):**
  - Non-IQ detector in a hybrid configuration with a CSI
  - Brute-force ADC or channel parallelization in Standards

- High-Q\_ L\_ Cavity CW-Operation:
  - at CMTB (DESY)

**Courtesy of L.Springer**

2020

2025?
Thanks for your attention!
2 eRTMs: Low Jitter RF and Clock Distribution

- Low-impedance bypass managed RF-Backplane

This avoids a complicated cable management.

- LO/CLK generation module
- Backplane manager
- Down-converter modules

<3fs, 1MHz BW (1.3GHz)

User slots for analog signals
### Content

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