Update on GigE Vision implementation in FPGA.

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Deutsches Elektronen-Synchrotron DESY
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ARD ST3 2019
> GigE Vision = protocol to transmit camera video over Ethernet
> implementation in FPGA → high-throughput, deterministic

Certification process
plugfest →
our implementation now certified

Come hear the stories from the plugfest!
10 GigE Vision

based on 10 Gigabit Ethernet → 10 times higher throughput

Two cameras with 10GigE Vision interface:

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<td>FLIR Oryx 10GigE</td>
<td>2448 x 2048</td>
<td>12</td>
<td>9746*</td>
</tr>
<tr>
<td>JAI SW-4000T-10GE</td>
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<td>10</td>
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Signal integrity on our platforms:

First tests successful, more work to do (wider datapath).

New HW platform

Already supported:
- DAMC-TCK7 (Kintex 7)
- Xilinx KCU105 eval kit (Kintex US)
- NAMC-ZYNQ-FMC (Zynq 7000)

New:
- Struck SIS8160

High memory throughput:
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Come see the poster!