LLRF Firmware of FERMI@ELETTRA

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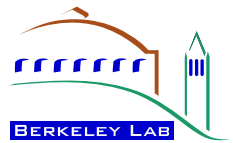
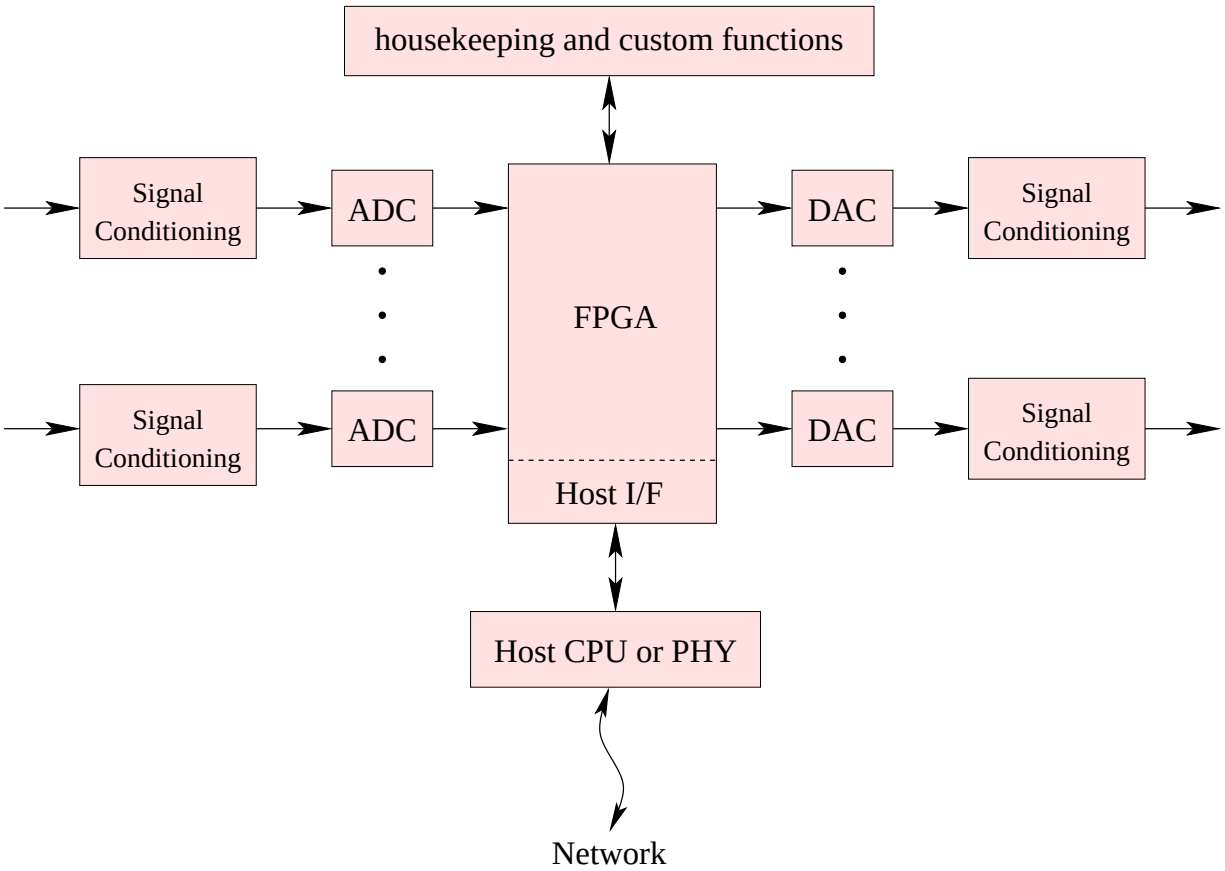


Low Level RF Workshop, Hamburg 2011

Representing:
LBNL: Gang Huang, Alessandro Ratti, John Byrd, Carlos Serrano,
Matt Stettler; Sincrotrone Trieste: Federico Gelmetti,
Massimo Milloch, Angela Salom, Alessandro Fabris;
TSR Engineering: Tony Rohlev

Outline

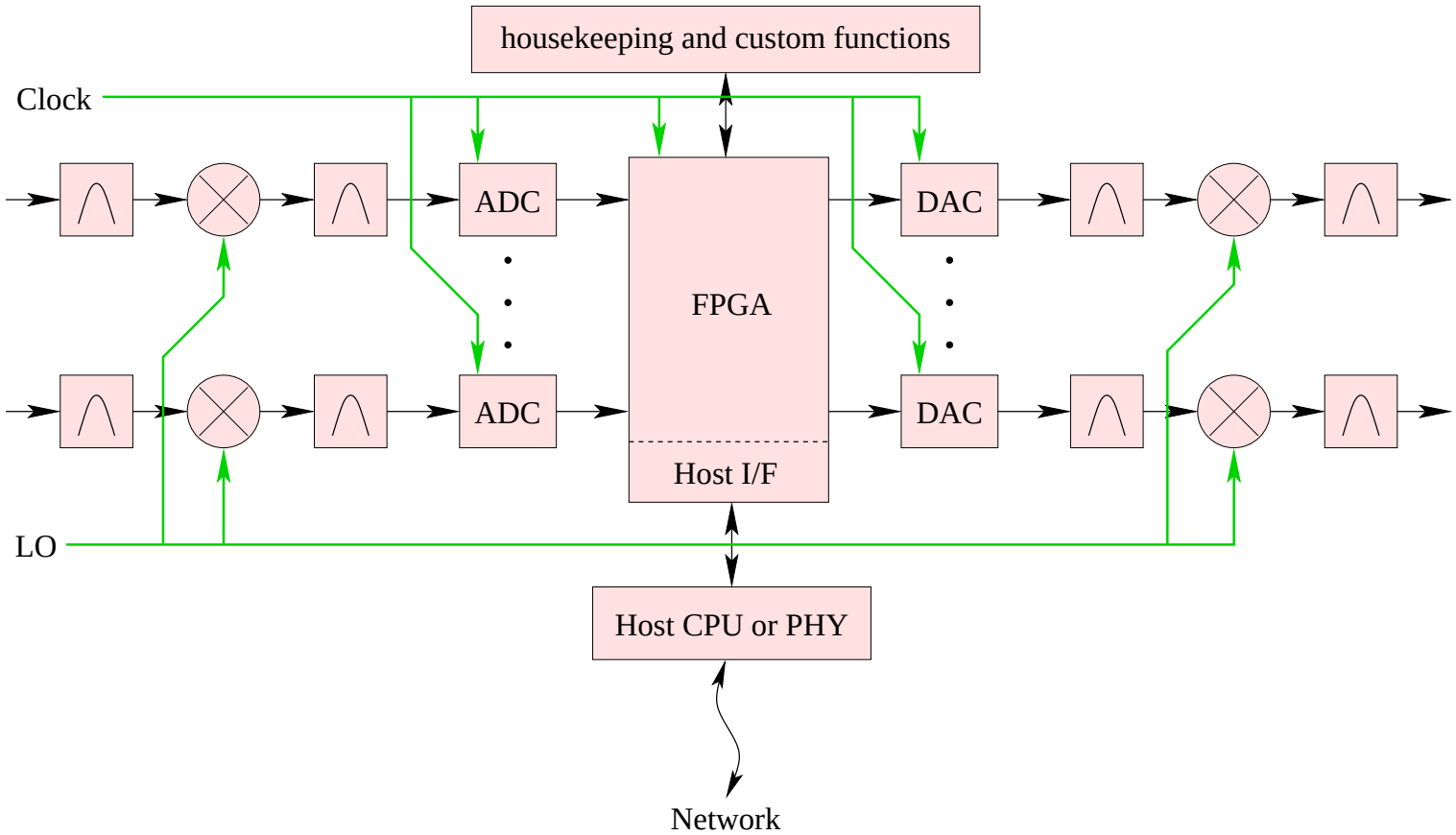
Familiar block diagram



"The cheapest, fastest and most reliable components of a computer system are those that aren't there."

- Gordon Bell (1934-), U.S. computer engineer

Familiar block diagram



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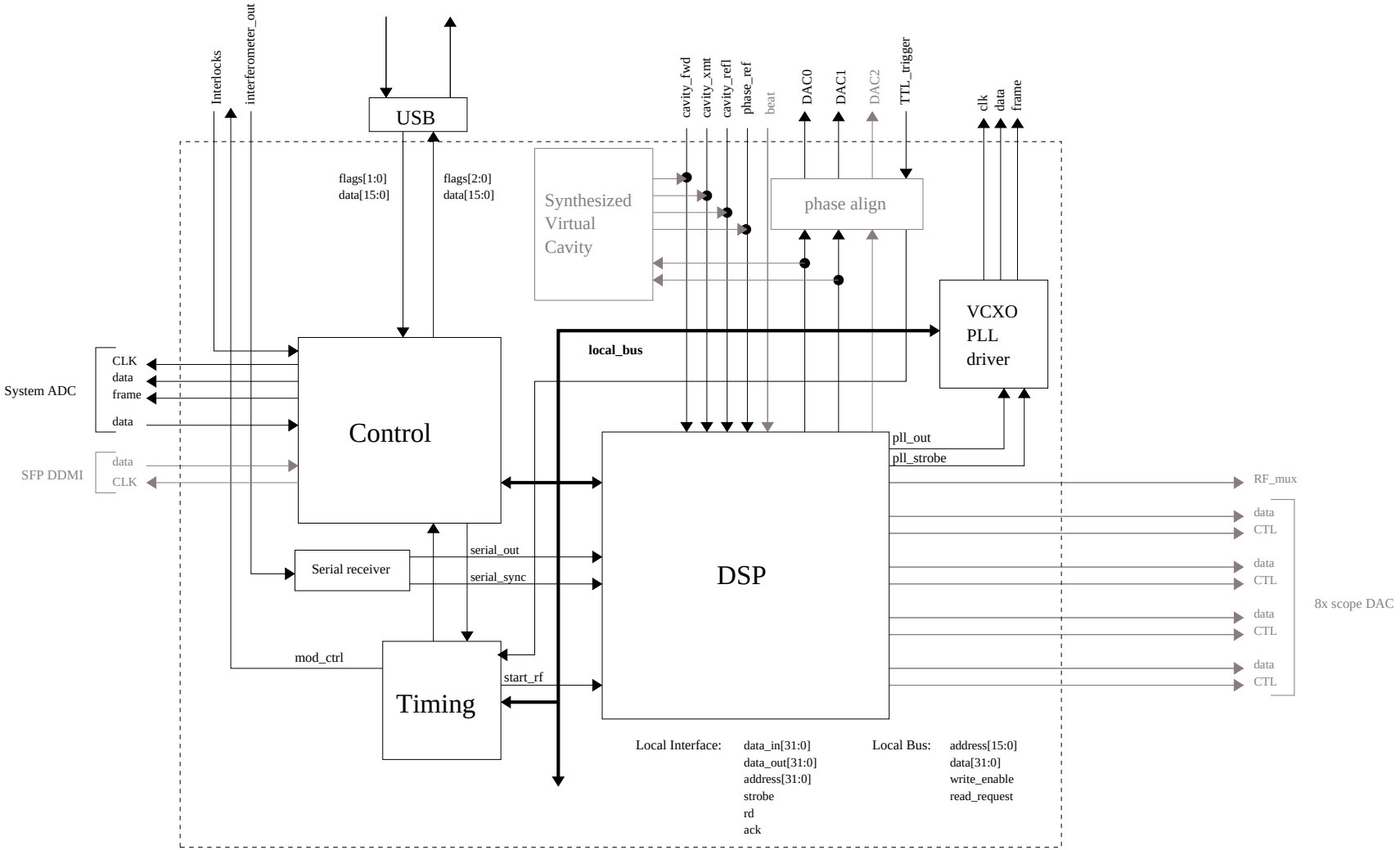
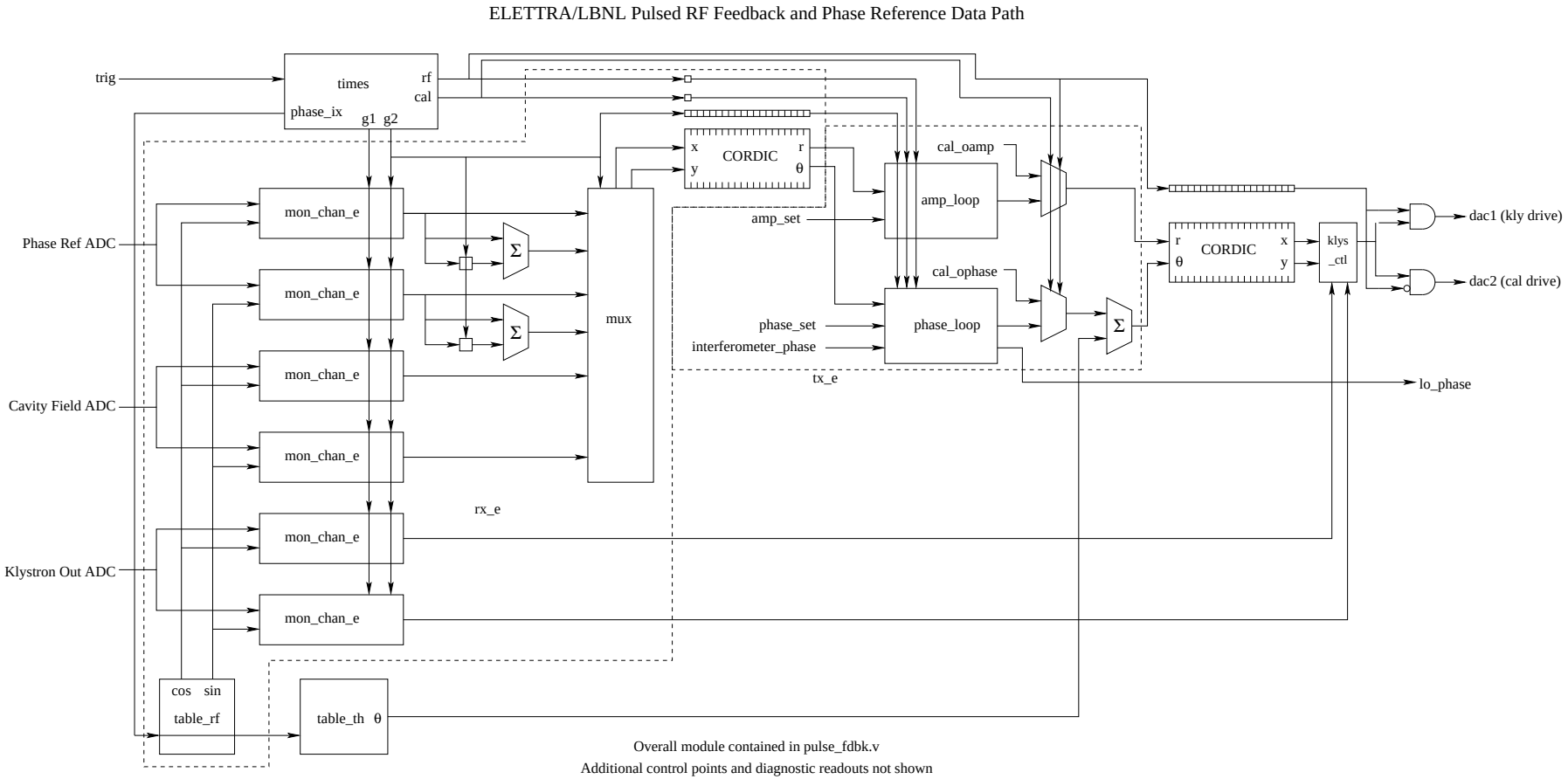
Overall Block Diagram



Core DSP Block Diagram

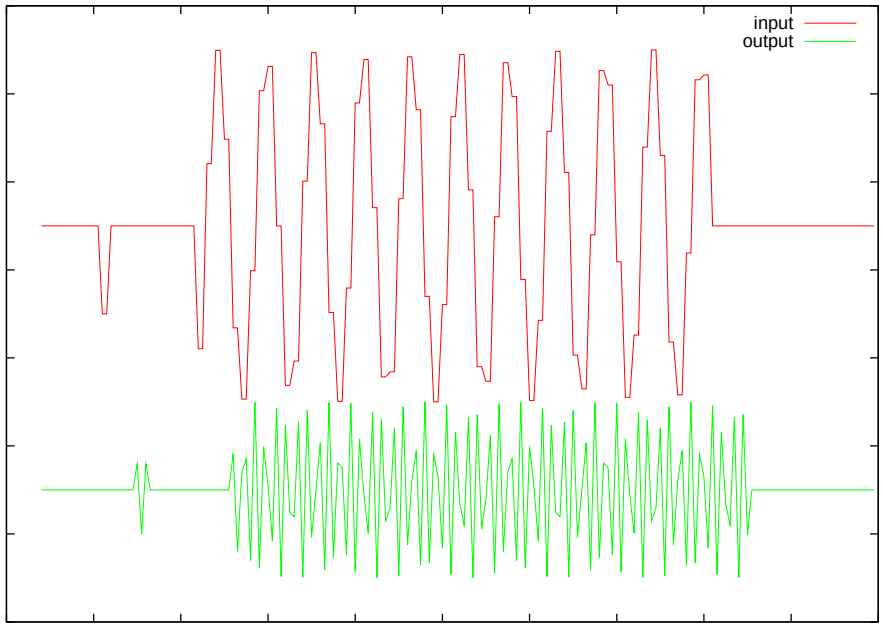


Good Simulation Environment

Unit test example: x2 interploator, tuned for 50/61*f_S

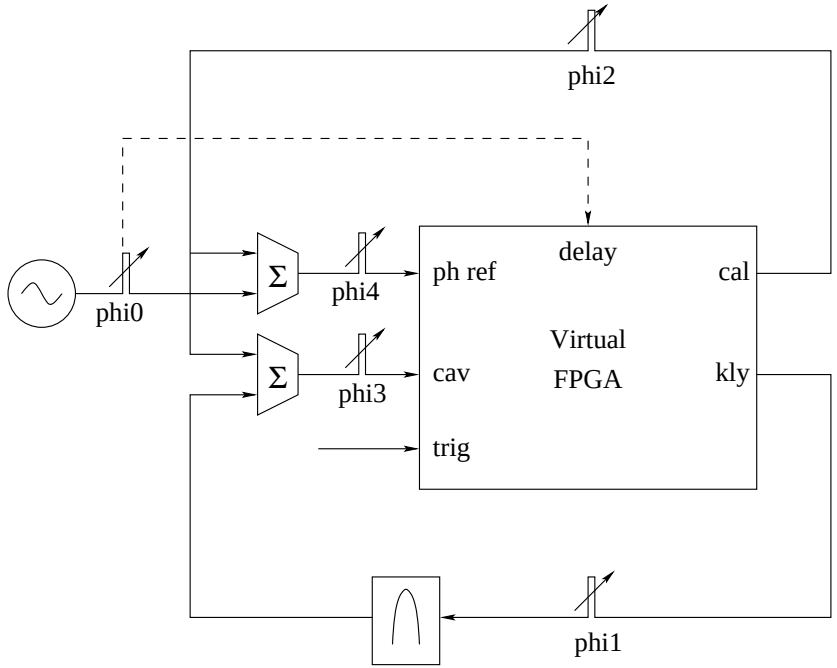
- 43 lines of synthesizable Verilog
- 66 lines of test bench Verilog
- test bench exercises impulse response, then a sine wave, checks that sine wave is interpolated with ± 1 bit error
- center frequency parameterized (used on other projects)

Normal output is boring: PASS; debugging graph:



Simulation fully exercises calibration scheme

```
   kly_old   ref   ref_cal   cav   cav_cal cal_out  pherr
 1 115.079 115.078 295.078 230.159 295.078 179.998 115.084 ignore
 2 359.999 115.078 295.078 115.079 295.078 179.998   0.004     OK
 3 359.999 115.078 295.078 115.079 295.078 179.998   0.004     OK
setpoint=100
 4  99.998 115.078 295.079 215.078 295.078 179.998   0.003     OK
 5  99.998 115.078 295.079 215.078 295.078 179.998   0.003     OK
 6  99.999 115.078 295.078 215.079 295.078 179.998   0.004     OK
phi1=20
 7  99.998 115.078 295.078 235.078 295.078 179.998  20.003 ignore
 8  79.998 115.078 295.079 215.078 295.078 179.998   0.003     OK
 9  79.998 115.078 295.079 215.078 295.078 179.998   0.003     OK
phi2=30
10  79.998 115.078 295.078 215.078 295.078 149.997   0.003     OK
11  79.999 115.078 295.078 215.079 295.078 149.998   0.004     OK
12  79.999 115.078 295.078 215.079 295.078 149.998   0.004     OK
phi3=45
13 124.998 115.078 295.078 305.079 340.078 149.998  45.004 ignore
14  79.998 115.078 295.078 260.079 340.078 149.998   0.004     OK
15  79.998 115.078 295.078 260.079 340.078 149.998   0.004     OK
phi4=70
16  80.002 185.083   5.083 260.083 340.083 150.002   0.008 ignore
17  80.002 185.083   5.083 260.083 340.083 150.001   0.008     OK
18  80.002 185.083   5.083 260.083 340.083 150.002   0.008     OK
phi3=55
phi4=80
19  90.000 195.081  15.081 280.081 350.081 150.001  10.006 ignore
20  80.001 195.081  15.081 270.082 350.082 150.001   0.007     OK
21  80.001 195.081  15.081 270.083 350.082 150.000   0.008     OK
phi0=45
22 124.999 240.080  60.080 315.081  35.081 195.000   0.006     OK
23 124.999 240.080  60.080 315.081  35.081 195.000   0.006     OK
24 124.999 240.080  60.080 315.081  35.081 195.000   0.006     OK
PASS
```



slow drift phase and amplitude, 5 places

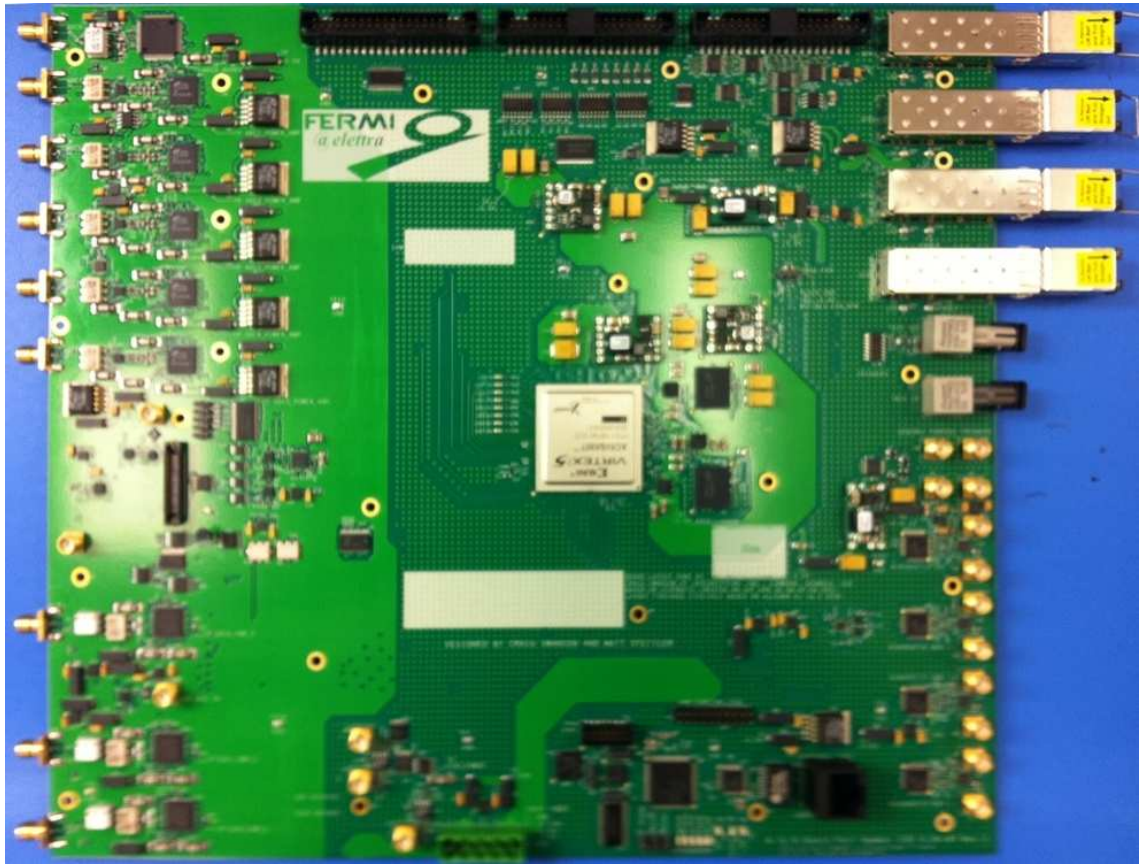
show cavity field held within tolerance

not included:

- LO phase lock
- serial comm and freq ratio multiply
- waveform acquisition and host interface

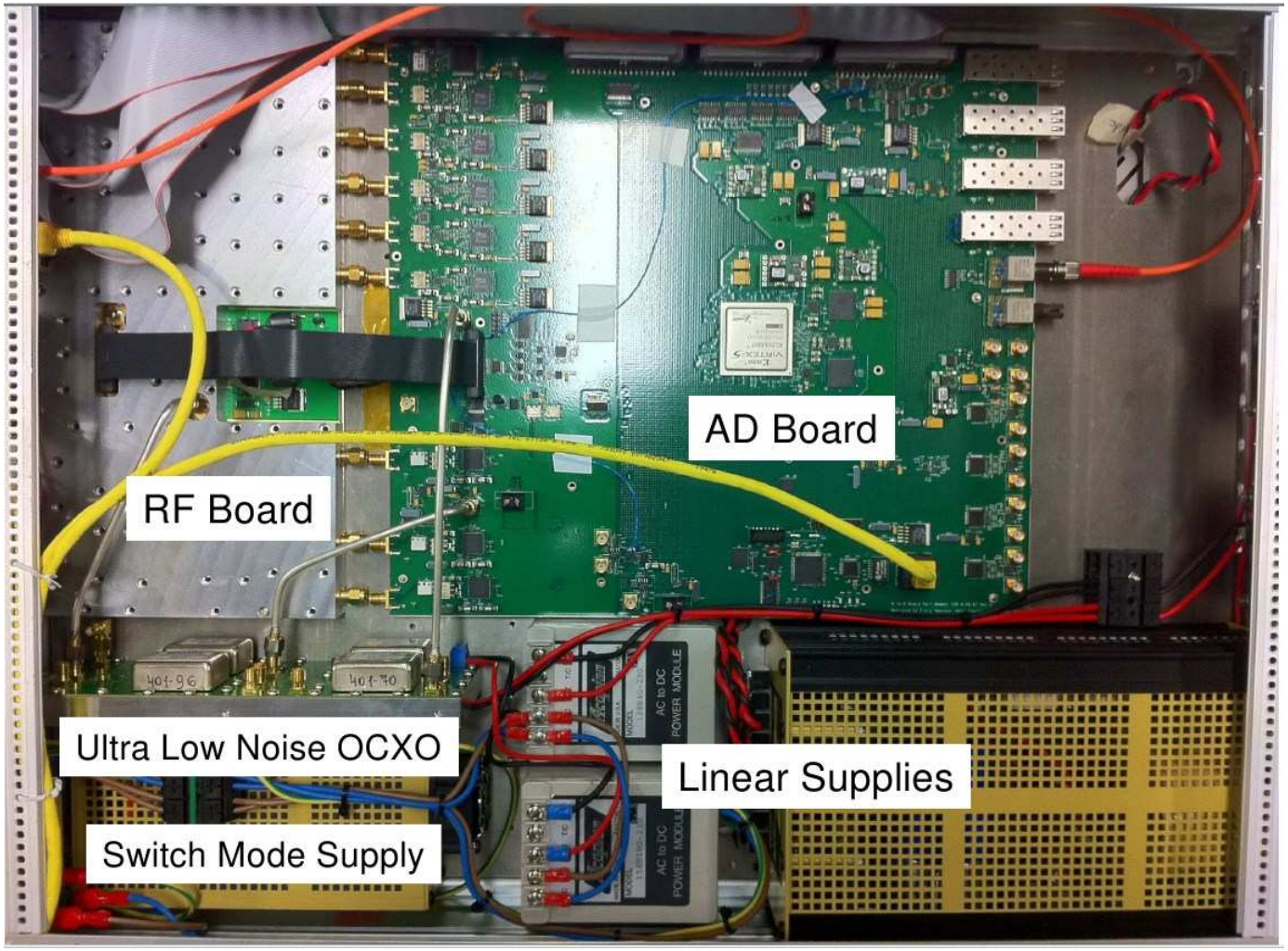
Hardware Platform

Pizza box, not crate; evolution of digital boards:



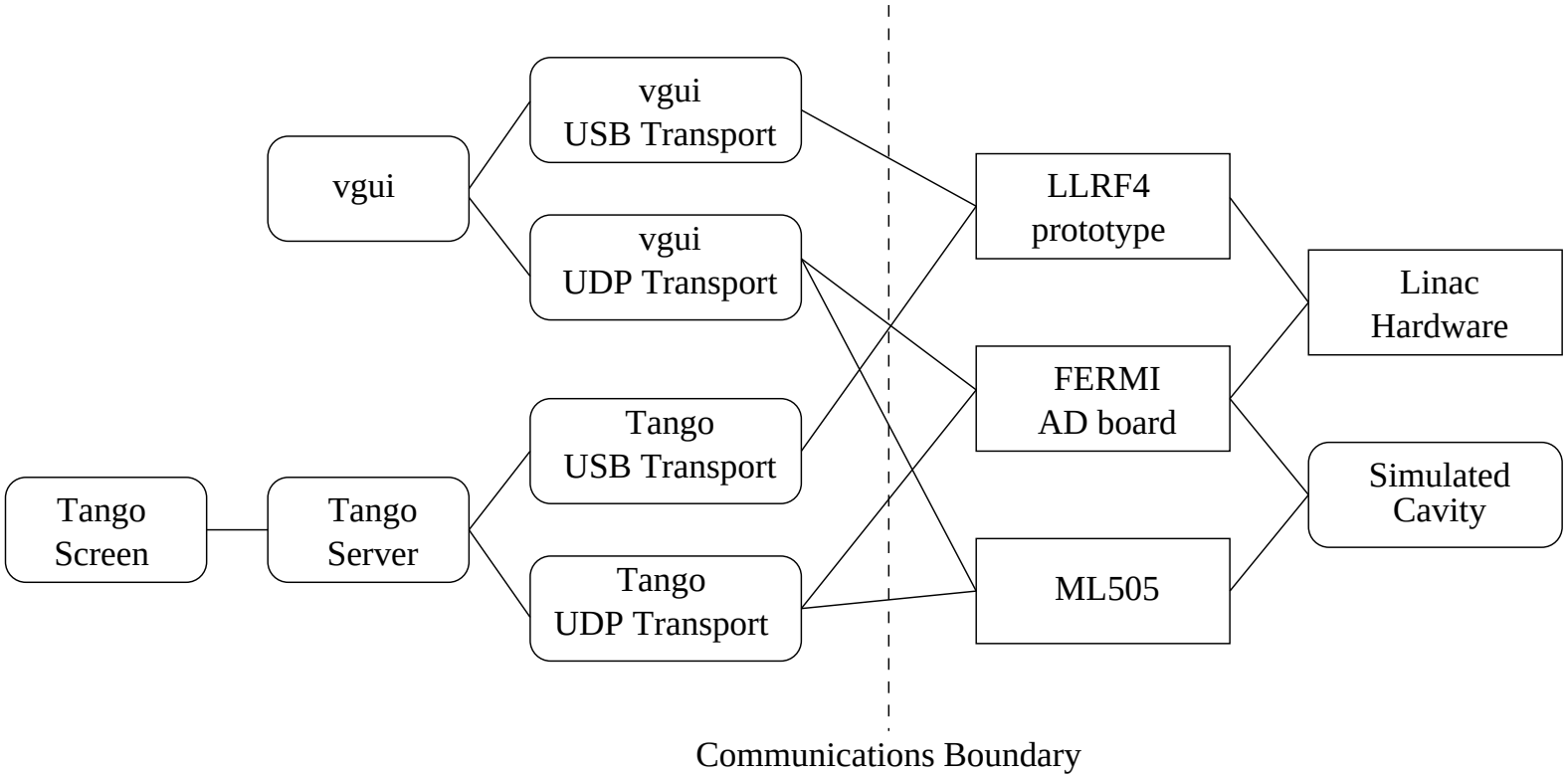
Density a better match than crate for one Klystron/cavity
Engineering focuses on actual RF tasks, not constraints inherited from other systems

Chassis (Pizza box)

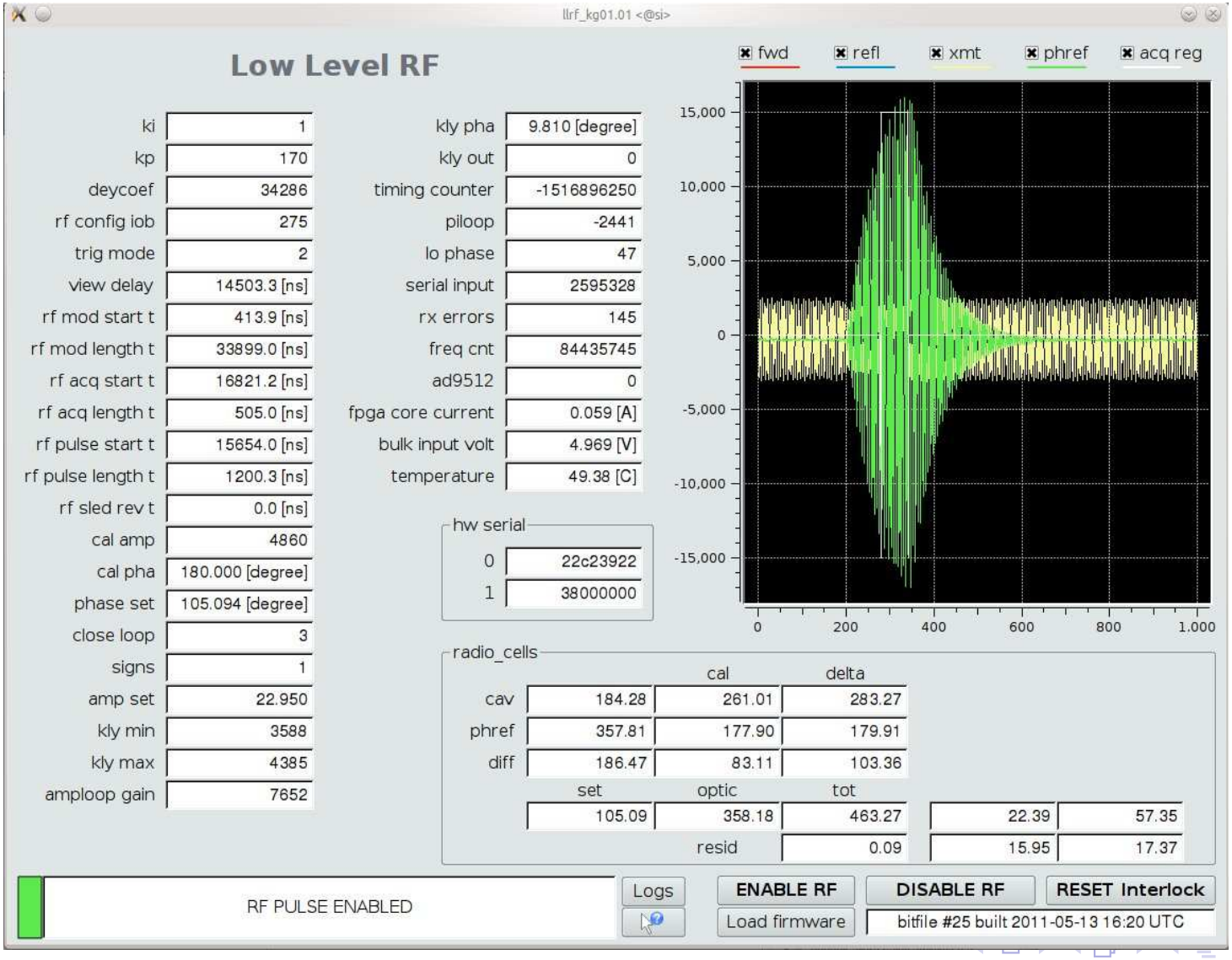


Assembled cost: ∼13 kEuro

Incremental Software System Tests



Operator Screen



System is in place and in use with beam
Production hardware is in testing now

Successful Gatware development requires

- clear concept of architecture and resource utilization
- simulations that represent reality, ideally pass/fail
- early connection to software

Vielen Dank!