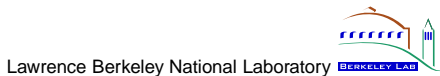


# LLRF Firmware of FERMI@ELETTRA

Larry Doolittle



Low Level RF Workshop, Hamburg 2011

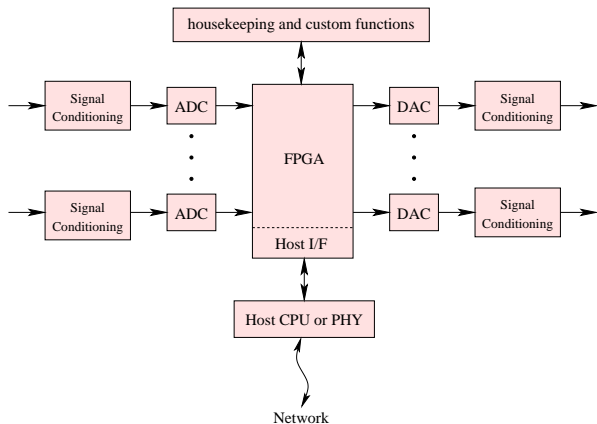
Representing:

LBL: Gang Huang, Alessandro Ratti, John Byrd, Carlos Serrano,  
Matt Stettler; Sincrotrone Trieste: Federico Gelmetti,  
Massimo Milloch, Angela Salom, Alessandro Fabris;  
TSR Engineering: Tony Rohlev

# Outline

- 1 Introduction and Context
- 2 Design and Simulation
- 3 Hardware and System Tests
- 4 Status and Summary

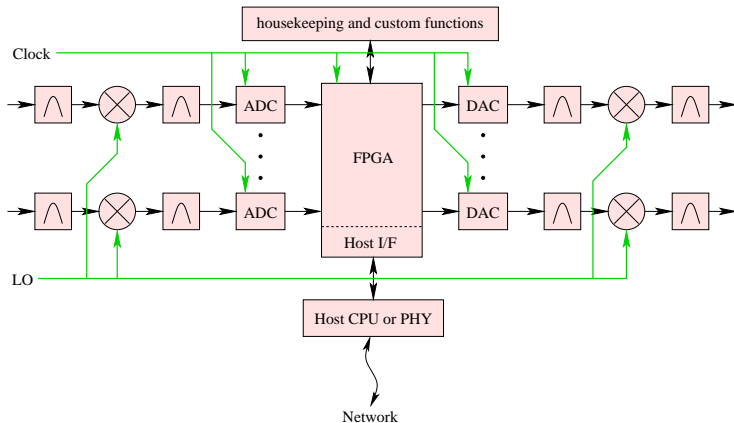
# Familiar block diagram



“The cheapest, fastest and most reliable components of a computer system are those that aren’t there.”

- Gordon Bell (1934-), U.S. computer engineer

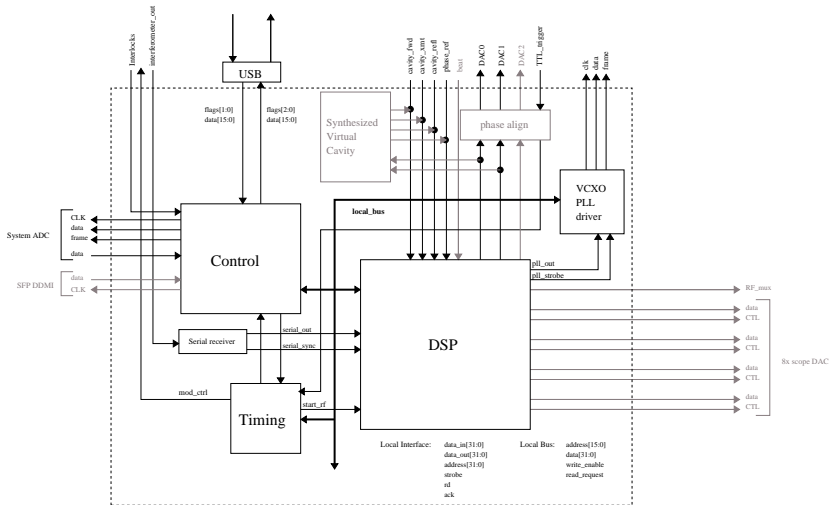
# Familiar block diagram



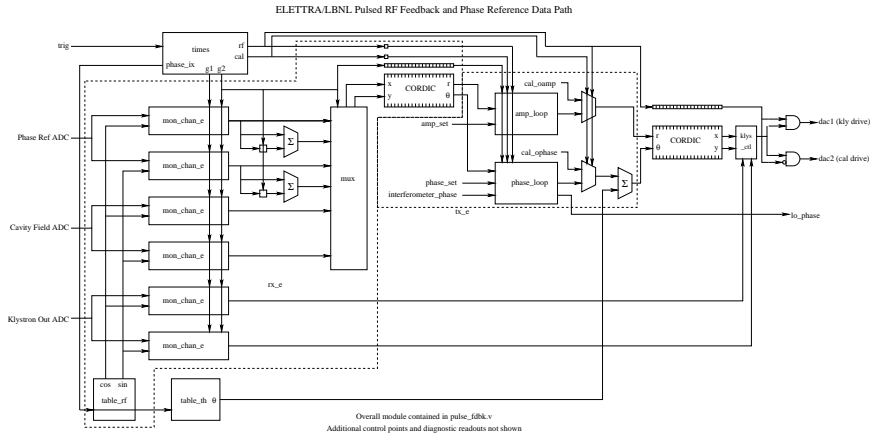
“The cheapest, fastest and most reliable components of a computer system are those that aren’t there.”

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# Overall Block Diagram



# Core DSP Block Diagram

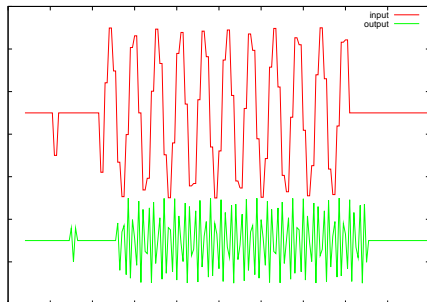


# Good Simulation Environment

Unit test example: x2 interpolator, tuned for  $50/61 * f_S$

- 43 lines of synthesizable Verilog
- 66 lines of test bench Verilog
- test bench exercises impulse response, then a sine wave, checks that sine wave is interpolated with  $\pm 1$  bit error
- center frequency parameterized (used on other projects)

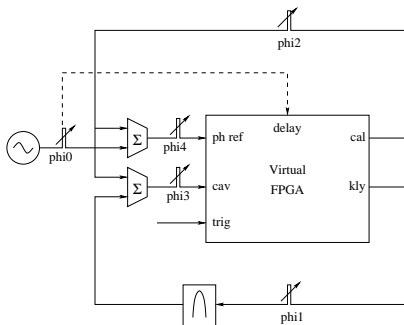
Normal output is boring: PASS; debugging graph:



# Simulation fully exercises calibration scheme

```

kly_old  ref  ref_cal  cav  cav_cal  cal_out  pherr
1 115.079 115.078 295.078 230.159 295.078 179.998 115.084 ignore
2 359.999 115.078 295.078 115.079 295.078 179.998 0.004 OK
3 359.999 115.078 295.078 115.079 295.078 179.998 0.004 OK
setpoint=100
4 99.998 115.078 295.079 215.078 295.078 179.998 0.003 OK
5 99.998 115.078 295.079 215.078 295.078 179.998 0.003 OK
6 99.999 115.078 295.078 215.079 295.078 179.998 0.004 OK
phi1=20
7 99.998 115.078 295.078 235.078 295.078 179.998 20.003 ignore
8 79.998 115.078 295.079 215.078 295.078 179.998 0.003 OK
9 79.998 115.078 295.079 215.078 295.078 179.998 0.003 OK
phi2=30
10 79.998 115.078 295.078 215.078 295.078 149.997 0.003 OK
11 79.999 115.078 295.078 215.079 295.078 149.998 0.004 OK
12 79.999 115.078 295.078 215.079 295.078 149.998 0.004 OK
phi3=45
13 124.998 115.078 295.078 305.079 340.078 149.998 45.004 ignore
14 79.998 115.078 295.078 260.079 340.078 149.998 0.004 OK
15 79.998 115.078 295.078 260.079 340.078 149.998 0.004 OK
phi4=70
16 80.002 185.083 5.083 260.083 340.083 150.002 0.008 ignore
17 80.002 185.083 5.083 260.083 340.083 150.001 0.008 OK
18 80.002 185.083 5.083 260.083 340.083 150.002 0.008 OK
phi3=55
phi4=80
19 90.000 195.081 15.081 280.081 350.081 150.001 10.006 ignore
20 80.001 195.081 15.081 270.082 350.082 150.001 0.007 OK
21 80.001 195.081 15.081 270.083 350.082 150.000 0.008 OK
phi0=45
22 124.999 240.080 60.080 315.081 35.081 195.000 0.006 OK
23 124.999 240.080 60.080 315.081 35.081 195.000 0.006 OK
24 124.999 240.080 60.080 315.081 35.081 195.000 0.006 OK
PASS
    
```

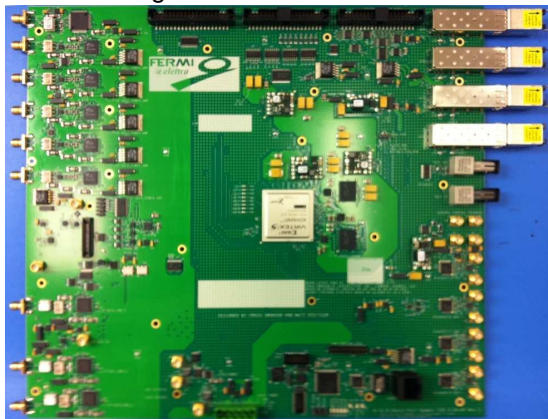


slow drift phase and amplitude, 5 places  
 show cavity field held within tolerance  
 not included:  
 LO phase lock  
 serial comm and freq ratio multiply  
 waveform acquisition and host interface



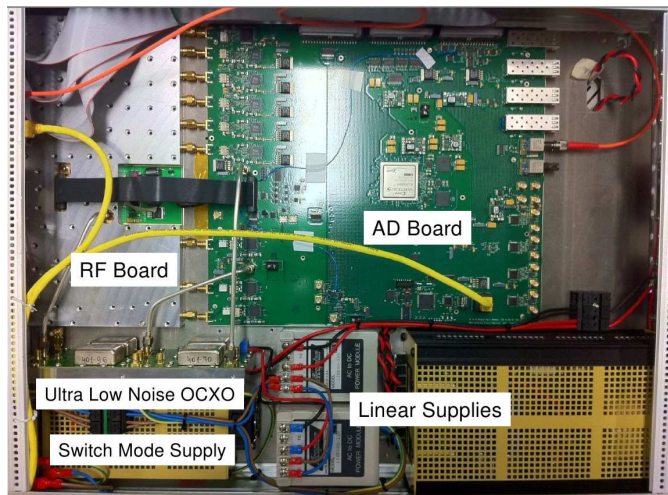
# Hardware Platform

Pizza box, not crate; evolution of digital boards:



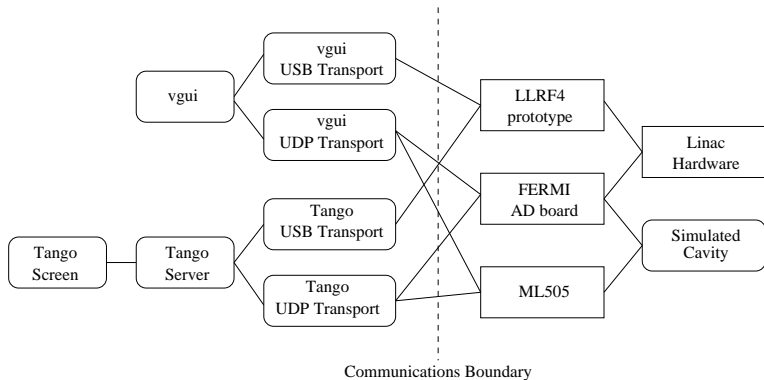
Density a better match than crate for one Klystron/cavity  
Engineering focuses on actual RF tasks, not constraints inherited from other systems

# Chassis (Pizza box)



Assembled cost:  $\sim 13$  kEuro

# Incremental Software System Tests



# Operator Screen

rf\_kg01.01 <@si>

## Low Level RF

ki	1
kp	170
deycoef	34286
rf config job	275
trig mode	2
view delay	14503.3 [ns]
rf mod start t	413.9 [ns]
rf mod length t	33899.0 [ns]
rf acq start t	16821.2 [ns]
rf acq length t	505.0 [ns]
rf pulse start t	15654.0 [ns]
rf pulse length t	1200.3 [ns]
rf sled rev t	0.0 [ns]
cal amp	4860
cal pha	180.000 [degree]
phase set	105.094 [degree]
close loop	3
signs	1
amp set	22.950
kly min	3588
kly max	4385
amploop gain	7652

kly pha	9.810 [degree]
kly out	0
timing counter	-1516896250
piloop	-2441
lo phase	47
serial input	2595328
rx errors	145
freq cnt	84435745
ad9512	0
fpga core current	0.059 [A]
bulk input volt	4.969 [V]
temperature	49.38 [C]

hw serial

0	22c23922
1	38000000

radio\_cells

	cal	delta
cav	184.28	261.01 283.27
phref	357.81	177.90 179.91
diff	186.47	83.11 103.36
set	105.09	358.18 463.27
resid		0.09 15.95 17.37

✕ fwd
✕ refl
✕ xmt
✕ phref
✕ acq reg

RF PULSE ENABLED

Logs

Load firmware

ENABLE RF

DISABLE RF

RESET Interlock

bitfile #25 built 2011-05-13 16:20 UTC

System is in place and in use with beam  
Production hardware is in testing now

Successful Gatware development requires

- clear concept of architecture and resource utilization
- simulations that represent reality, ideally pass/fail
- early connection to software

**Vielen Dank!**