LLRF 2011

LLRF Controller Implementation for uTCA based LLRF System

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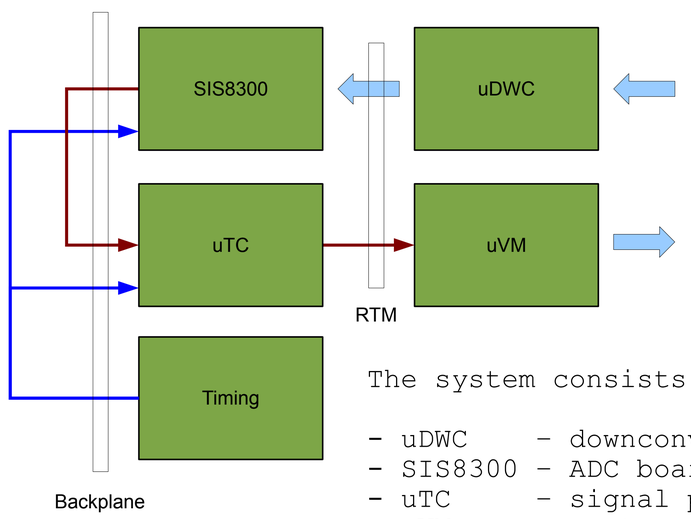
Hardware System Structure



Boards are equipped with 2 communication channels:

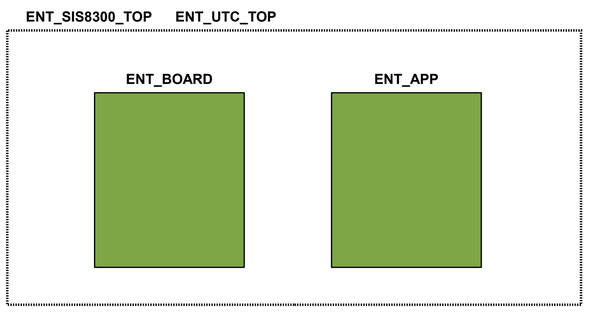
- PCIe
- LLL (Low Latency Link)

The system consists of the following boards:

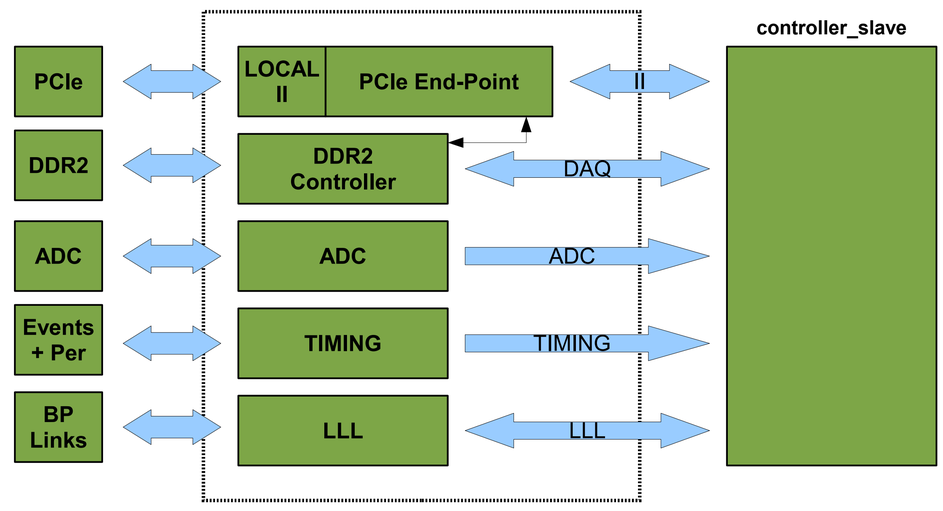
- uDWC – downconverter board with IF 54MHz
- SIS8300 – ADC board
- uTC – signal processing board
- uVM – vector modulator board
- Timing – event decoder and distributor

BSP Firmware Framework

Special firmware framework has been prepared to unify structure for all boards. The top level structure has been divided into BOARD specific part (peripheral drivers, communication modules, etc.) and APPLICATION specific part (processing algorithm, etc.)

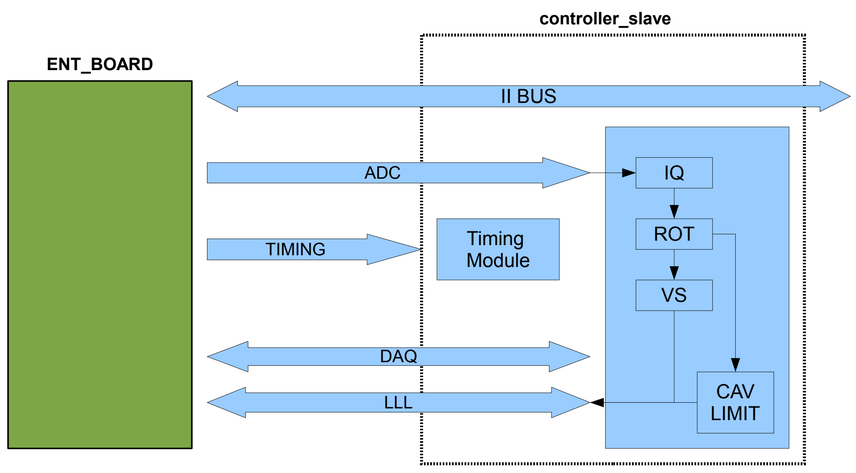


The sample structure of the BOARD part is presented below.



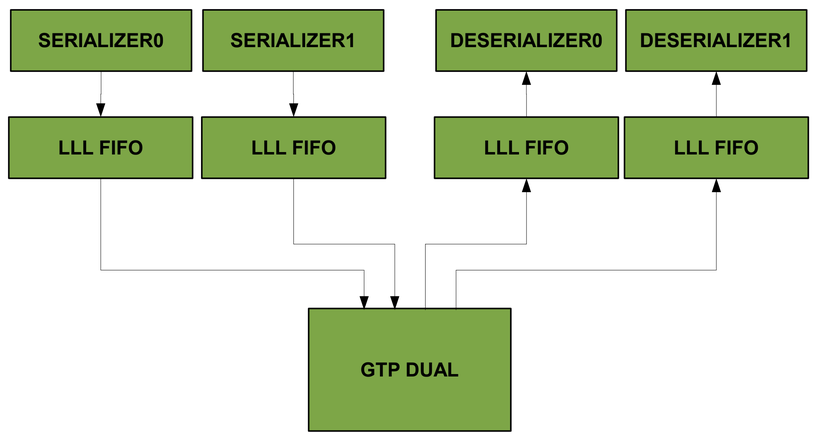
SIS8300 controller_slave application

SIS8300 is responsible for field detection for individual channels and for vector sum calculation. It is transmitted to uTC board for further calculations.



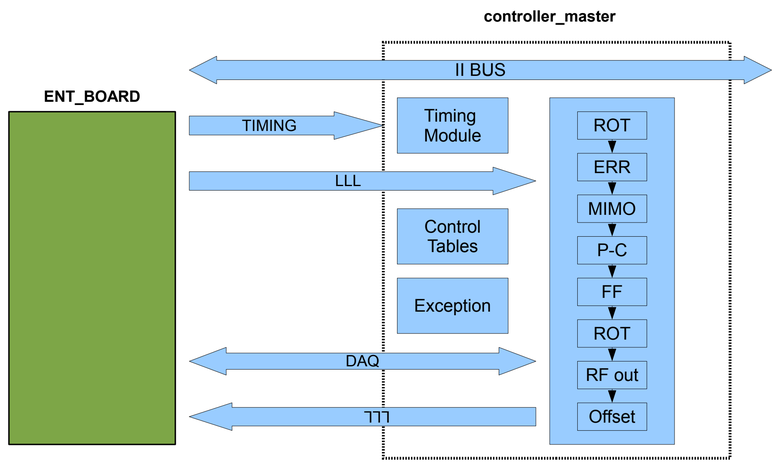
Low Latency Link Module

Special LLL module has been prepared to provide fast, high bandwidth connections between algorithm stages implemented on different boards. It utilizes GTP_DUAL embedded SERDES. Structure is presented below.



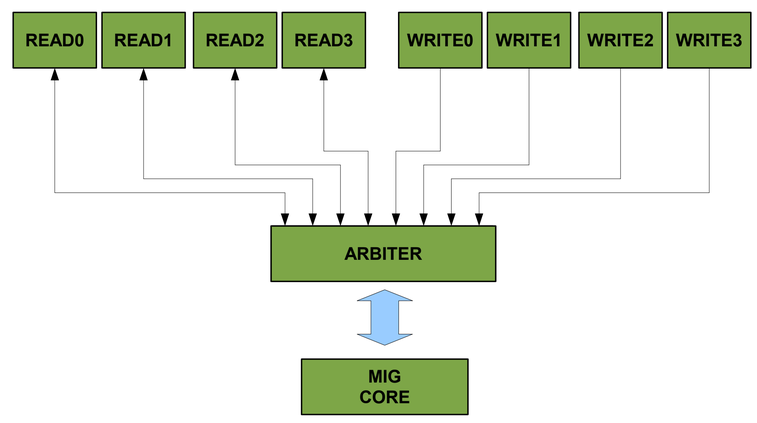
uTC controller_master application

UTC board is responsible for control algorithm execution. It processes vector sum received from SIS8300 to calculate final control signal, which is transmitted to uVM.



Memory Controller

To provide memory access for all necessary clients (PCIe DMA transfers, DAQ subsystem, CTL subsystem) special multiport memory controller has been prepared. It is based on MIG core extended by 8 port customizable arbiter.



ADC clocking considerations

To utilize full 125MHz sampling rate special design consideration must be taken into account. The diagram presents usage of special clock buffers.