# VECTOR MODULATOR CARD FOR THE µTCA BASED LLRF CONTROL SYSTEM

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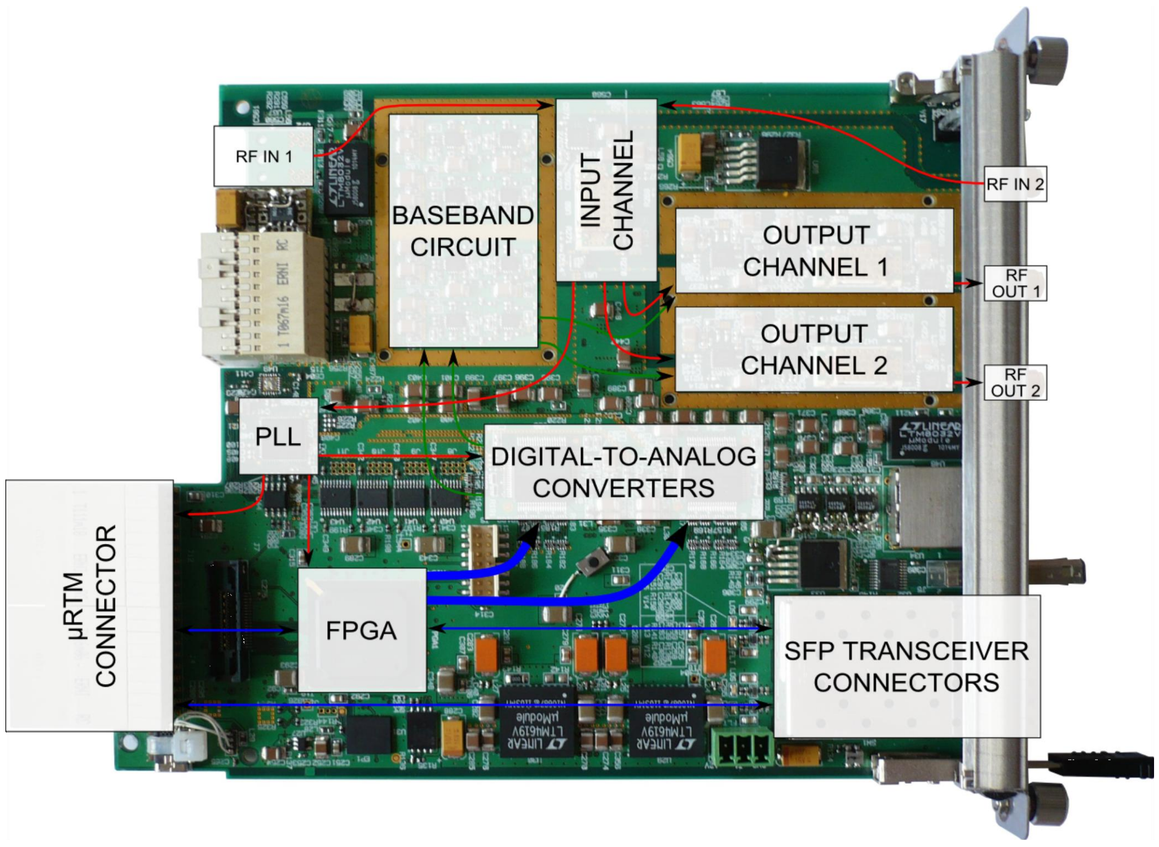
## Introduction

The LLRF control system for FLASH and European XFEL require fast, high-resolution Vector Modulator module (µVM) realized in the µTCA standard. The µVM was designed to be used as a µRTM module of µTCA based Controller (µTC). It offers two independent IQ modulator channels covering input frequency range from 100 MHz to 4 GHz. The output power is controlled by an adjustable attenuator, hence the resolution of operation is not compromised when reducing the output power level. The analogue RF-chains have also build in power monitoring capabilities. The digital part of the board offers a variety of control and data interfaces including high-speed serial links and equalized LVDS parallel buses to µTC module.

## Board Concept

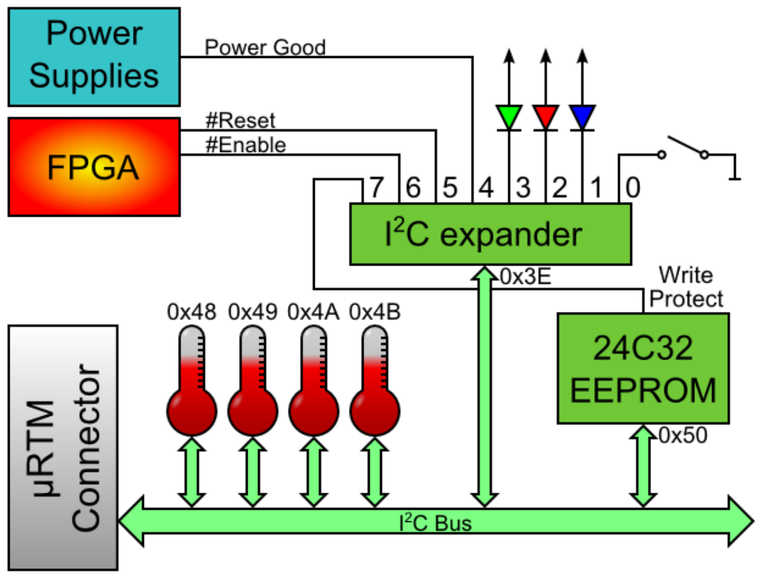
- The FPGA used to control the board features and provide communication via fast links
- Two independent dual DACs to control both modulator channels
- Baseband circuit with low noise amplifiers and filters for DAC output signal conditioning
- The RF input switchable between the RF backplane and the SMA connector on the front panel
- RF channel outputs via two SMA connectors




**The µVM module functional components**

## RTM Module Management

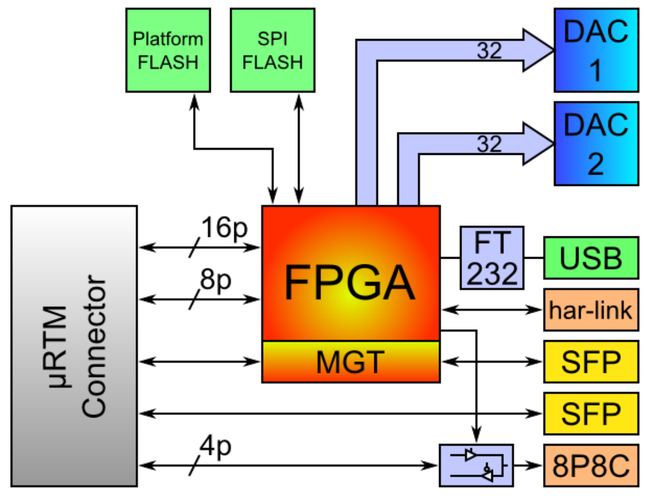
- Basic management module required by MTCA.4 draft specification
- Reading of hot-swap sensor, driving optical indicators and monitoring of power supply good signals
- Two-wire interface to the FPGA and controls the 'write protect' signal of the on-board serial EEPROM memory
- EEPROM used to store information of µRTM module capabilities
- Digital thermometer circuits are placed in the most critical parts of the PCB




**Module management and health monitoring of VM**

## Digital Subsystem of the µVM

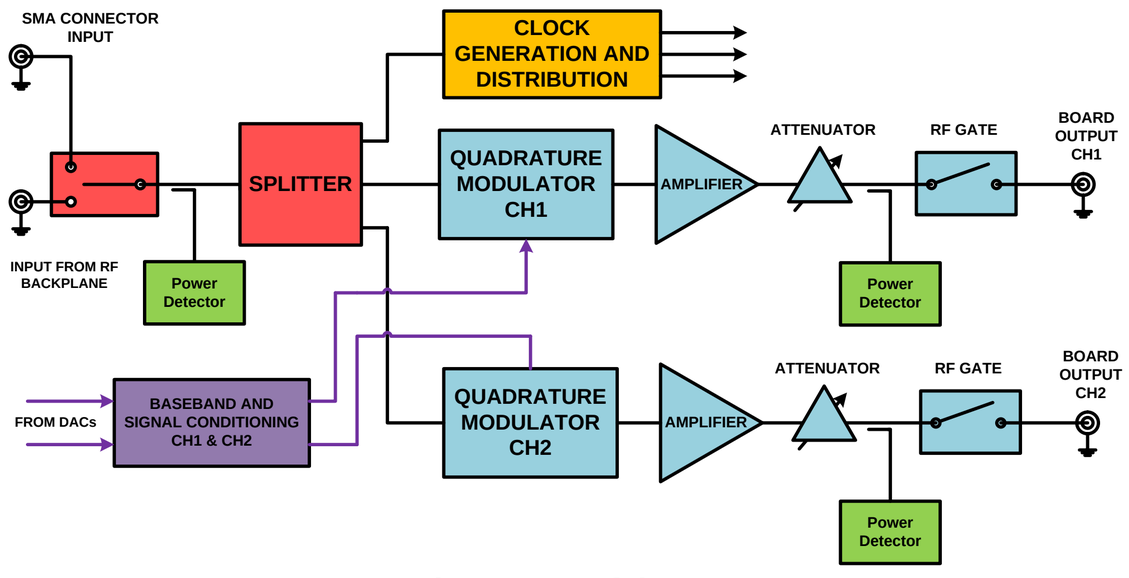
- Provides communication interface to the LLRF controller
- Assures module configuration and management
- Low latency serial gigalink or LVDS parallel bus to µTC
- The µVM FPGA controls main DACs, clock distribution circuit, attenuators, RF power monitoring circuit, monitoring ADC, base-band DAC using seven independent SPI buses
- Har-link connector and USB emulated serial port
- FPGA configuration by FLASH memory. FLASH memory and FPGA are directly accessible using the JTAG interface
- Two dual 16-bit, 160 MSPS DACs are driven by parallel interfaces




**Block diagram of the digital subsystem of the µVM**

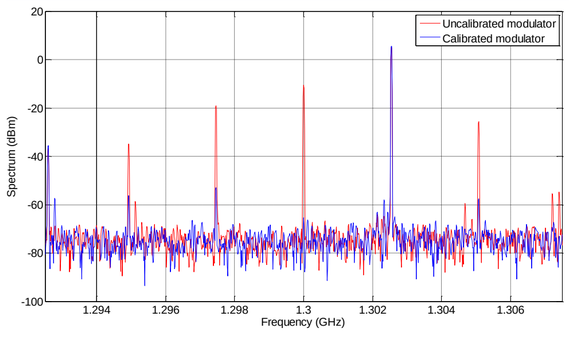
## Analogue Subsystems of the µVM

- Signal input can be selected by software
- Low jitter clocks generated from RF input signal
- Baseband signal circuits limit the analog bandwidth to 30 MHz
- Output power level range: -5 dBm to +10 dBm
- Programmable attenuator 0 to 15 dB of attenuation
- Output RF gate for interlock purposes
- Board can be configured to operate at various frequencies by selected RF components.
- Output signal phase noise floor of -160 dBc




**Analogue part of the µVM**

## Tests and Summary




| Harmonic | -3 | -2 | Unwanted sideband | Carrier | Wanted sideband | 2 | 3 |
|---|---|---|---|---|---|---|---|
| Power level (dBm) without calibration | -36.8 | -34.9 | -19.1 | -10.5 | 5 | -25.6 | -54.8 |
| Power level (dBm) with calibration | -35.7 | -56.2 | -53.0 | -65.4 | 5.5 | -57.5 | -73.0 |

**Measurement results of harmonic spectrum with 2.54MHz modulation @ 1.3G Hz. Achieved carrier suppression of 70.5 dB (after calibration)**

The µVM boards were tested at 1.3 GHz and 3.0 GHz in laboratories at the Warsaw University of Technology, Technical University of Lodz and in DESY. Achieved performance fulfills data provided in component datasheets. The board was sucessfully used during tests of the LLRF control system of FLASH accelerator in July and August 2011.

Several ways of improving of the µVM performance were found during tests and second board revision is planned.

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