Modelling, control design and simulation of a klystron amplifier at ESS-Bilbao

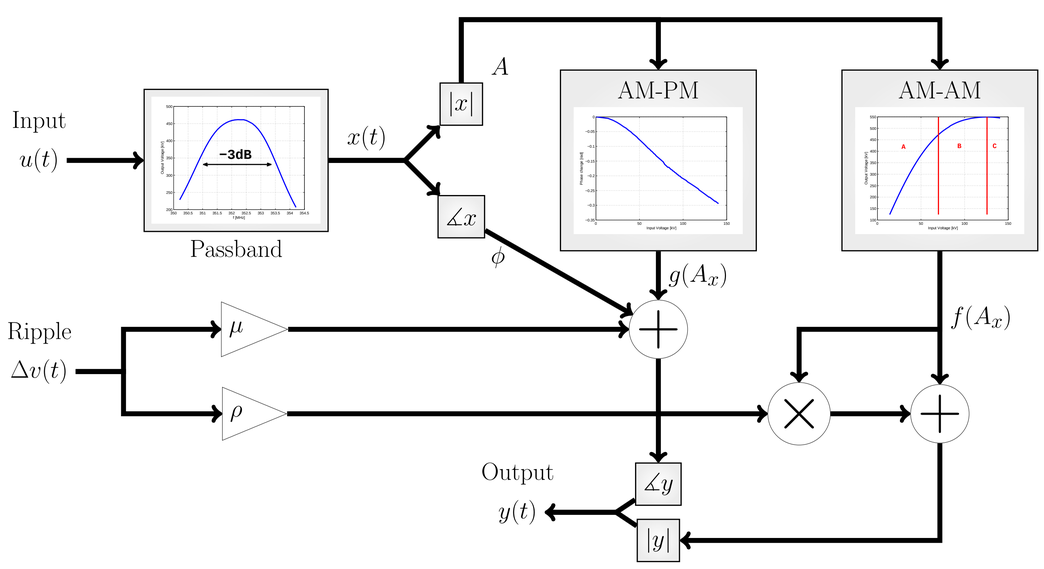
Tomaso Poggi, Hooman Hassanzadegan, Nagore Garmendia, Leire Muguira, Jordi Verdú, Joaquín Portilla

ESS-Bilbao, RF Systems Group, Bilbao, Spain

Abstract

The ESS-Bilbao (ESSB) light ion linear accelerator has been conceived as a multi-purpose machine, useful as the core of a new standalone accelerator facility in southern Europe giving support to local beam users and accelerator physicists. The project aims to develop significant in-house capabilities needed to support the country participation in a good number of accelerator projects worldwide.
In this context, the Low Level RF (LLRF) system plays a key role in the performance of an accelerator. A LLRF system typically consists of amplitude, phase and tuning loops to regulate the amplitude/phase of the RF field and the resonance frequency of the cavity respectively. While the amplitude and phase loops provide the necessary conditions for beam acceleration and focus, the tuning loop acts on the cavity tuner to keep the reflected power minimized thus avoid unnecessary power losses and saturations. Although LLRF systems are characterized by these three regulation loops, they also include a control loop to regulate the klystron output and compensate its intrinsic nonlinear response. Thus, understanding and modelling the dynamics of a klystron amplifier is a pivotal step to design a LLRF system.
We present a behavioural dynamical model of a klystron amplifier and the related design of a PID based digital control system. The proposed model for the klystron amplifier is able to reproduce the main dynamics behaviour of a real klystron while keeping a reasonable degree of simplicity. Such a model can be used to reproduce non-linear input-output effects like saturation and phase mismatch. A particular klystron that can provide 3MW of peak output power at a frequency of 352MHz, 3MHz of bandwidth, has been considered. Free parameters have been identified from data provided by the klystron producer (Communications and Power Industries, CPI). In particular, AM-AM and AM-PM curves have been modelled with polynomials whose coefficients have been found by standard identification techniques (least squares).
Modern designs implement most of the signal processing on digital platforms, thus reducing the size and cost of the hardware. As a consequence it is interesting to provide tools and methods to design digital control algorithm that can be executed on programmable logic devices, such as FPGAs. A PID control system has been designed and implemented on FPGA in order to follow an input reference RF signal and to reject disturbances, mainly due to beam voltage ripple. A limiter and an anti-windup scheme have been also included to prevent the klystron to work in over-saturation zones, which is characterised by a low input/output gain.

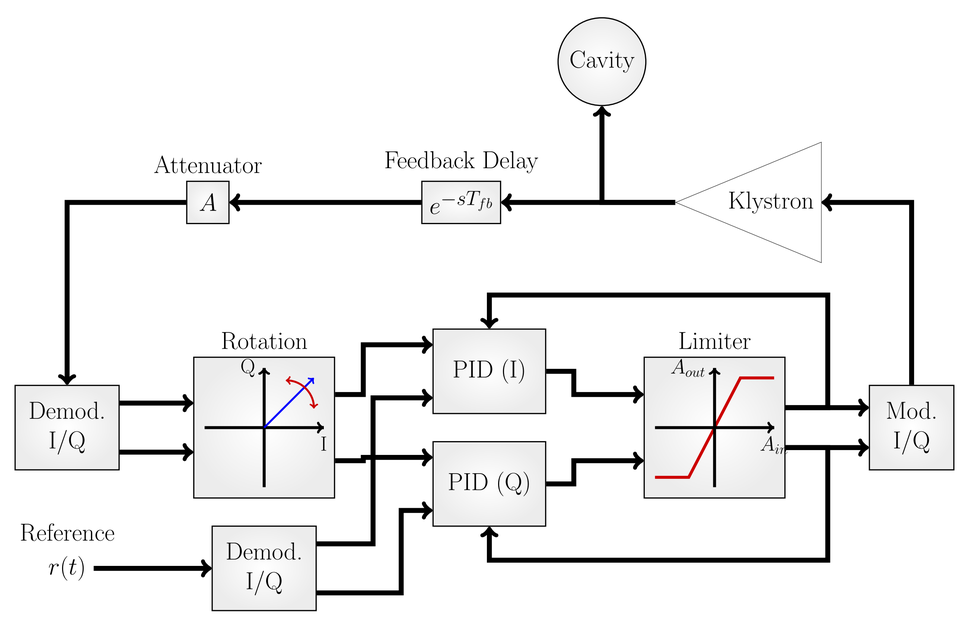
Klystron model



The model takes into account several aspects:

RF Input	$u(t) = A\cos(\omega t + \phi)$
	$\Downarrow$
Frequency response	$x(t) = A_x\cos(\omega t + \phi_x)$
	$\Downarrow$
AM-AM and AM-PM input-output relations	$f(A_x)cos(\omega t + \phi_x + g(A_x))$
	$\Downarrow$
Beam voltage ripples	$y(t) = (1 + \rho\Delta v)f(A_x)cos(\omega t + \phi_x + g(A_x) + \mu\Delta v)$

Control system



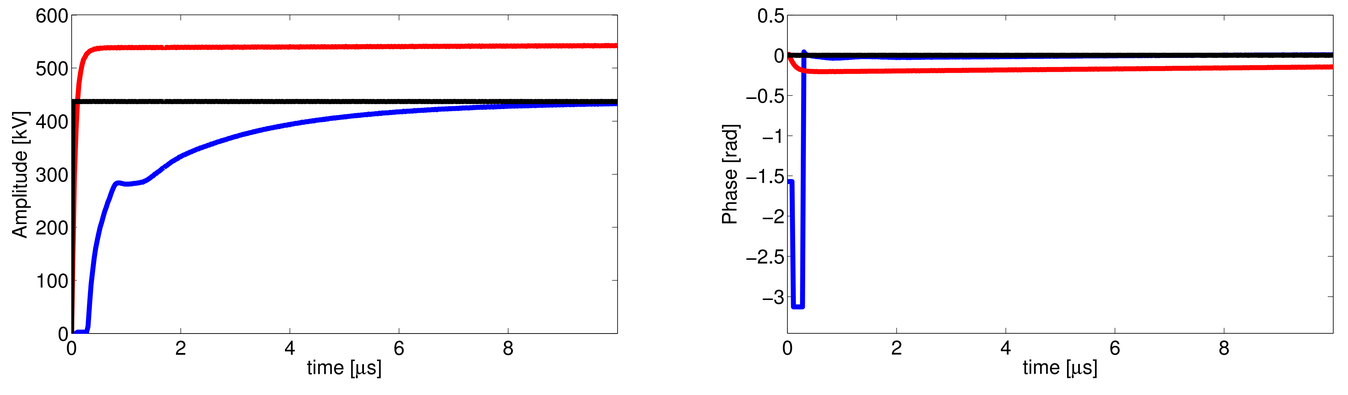
- Demodulation: the RF signal is demodulated to obtain its in-phase (I) and quadrature (Q) components;
- Phase compensation: the I-Q components are rotated to compensate the delay introduced by the feedback path;
- PID: The pair I-Q is passed to two different PID blocks;
- Modulation: the I-Q components are up-converted by a modulator to produce a RF signal.

Simulation and implementation results

Klystron parameters		
Type	Value	Unit
Frequency	352.2	MHz
Bandwidth $(-3dB)$	3	MHz
RF pulse width	1.5	ms
Peak power	3	MW
Beam voltage	110	kV
Beam voltage ripple	< 5	kV
Reference resistance	50	Ω

Specifications		
Type	Required	Obtained
Amplitude stability	1%	0.5%
Phase stability	1°	0.79°
Rise time	$\ll 300\mu s$	$6\mu s$

Reference **Open-loop response** **Close-loop response**



The parameters of the PID have been found analytically by taking into account the dynamics of the proposed klystron model. The control system has been implemented and tested on a Xilinx Virtex-IV FPGA, programmed through the Xilinx System Generator for DSP tool. Simulation results, obtained using Matlab/Simulink and the hardware-in-the-loop (HIL) technique, show that a reference RF signal can be tracked with an maximum amplitude error of 0.5% and a maximum phase error of 0.79°, even in the presence of beam voltage ripple.