MTCA Workshop for Industry and Research

Precision analog measurement in high speed MTCA.4 crates

Dr. Frank Ludwig
for the LLRF Team
Outline

> Motivation
> Receiver Performance
> Signal Integrity in MTCA.4
> Precision analog Measurements in MTCA.4
> Summary
Analog meets Digital in the MTCA.4 Crate

> Todays available ADCs

![Image of ADCs]

Figure 1: AD9066 and AD9069 Family Evaluation Board and HMC-ADC EVK32X Data Capture Board

Performance maintained?

\[
e_n = \frac{V_{FS,pp}}{\sqrt{8}} \times 10^{\frac{SNR(f_s, e)}{20}} \times \sqrt{\frac{2}{f_s}}
\]
Receiver Performance: 1 DUT Characterization

- Receiver subsystem noise contributions: noise balanced
  - Front-End
  - LO-Generation
  - ADC (limitation)

-150dBC/Hz

\[ \Delta \frac{A}{A} = 0.003\% \]

\[ \Delta P = 0.002^\circ \]

\[ \Delta f = 2.177 \times 10^{-4} \]

\[ < 0.0018 \text{, } 4\text{fs} \]

Receiver Performance: 1 DUT Characterization

- 1.3GHz

\[ A, \Delta \varphi \]

- Single Channel Field Detector
- AC-coupled
- \(-147\text{dBC/Hz (16-Bit ADC)}\)
- \(-150\text{dBC/Hz}\)

- Master-Oscillator
- Reference
- \(-150\text{dBC/Hz}\)
- Intermediate frequency [10MHz-50MHz]
- Sample frequency [50MHz-130MHz]
- ADC clock

- Non-IQ Sampling
- CIC Filter
- Digital IQ-Detection
- Input Calibration

- RF-Input
- LO-Input
- AC-coupled
- ADC

- Sample frequency [50MHz-130MHz]
- Single Channel Field Detector
- Input Calibration

Signal Integrity: Grounding Configurations in MTCA.4

- AMC-sided Analog section

- RTM-sided Analog section

- RTM/AMC-sided Analog section

  Mixed-mode design to be investigated.
Ground pollution due to connections … + internal distortions from

- Power supply,
- MCH+CPU+SSD+AMC+Timer1 …

Chassis-to-GND Spectrum

Depends on your input circuit CMR and requirement

Control of inner and forced currents of the crate
Ground distortion current paths and its reduction

- Reduce source of distortions (e.g. power supply)
- Bypass external distortions into the chassis
- Control return-currents from other ADCs (TBD)

Couple into single-ended inputs

Bypass via SMA screw

Bypass via FBM solder, SMA screw

ESD-Strip

Spurious free signals

Session 5: P. Goettlicher
"EMI challenges for a mixed mode usage of MTCA.4"
Requirements for the cavity field stability (long- and short-term):

Amplitude and Phase stability: $f_{CAV} = 1.3\, \text{GHz}$

- $\Delta A / A_{rms} = 0.01\%$, $\Delta \phi_{rms} = 0.01\, \text{deg}$
- $\Delta A / A_{rms} = 0.03\%$, $\Delta \phi_{rms} = 0.03\, \text{deg}$
- $\Delta A / A_{rms} = 0.1\%$, $\Delta \phi_{rms} = 0.1\, \text{deg}$

20fs @ 1.3GHz results in 4um cable length change

- Review meeting 12.2007: XFEL will be based on xTCA
- XFEL fast electronics will be based on MTCA.4: > 200 crates
High frequency regulation (simplified):
Subversions for:
- Injector linac
- Third harmonic
- NC structures
- Booster, main linac

ADC board for readout of:
- Probe signals
- Forward signals
- Reflected signals
- .....
- Control DCM / DWC

Courtesy of J. Branlard
LLRF System Performance Test at FLASH using MTCA.4

FLASH operation:

On-crest energy stability (SR-3BC2)

Energy stability dE/E = 5E-5.

Drift-Calibration Module (DCM)
Reference Module (REFM)
Local Frequency Generation (LOGM)

LLRF MTCA.4 Prototype System ACC1'
External Power Supply (PWSM)
REGAE (Relativistic Electron Gun for Atomic Exploration):
- Electron source for time resolved diffraction experiments

3GHz LLRF system based on MTCA.4:
- Buncher Cavity and RF-Gun S-Band, NC
- 10 channel process Kly/Gun/Buncher/Laser
- Non IQ IF=25MHz, fs=125MHz, LFF
- \( dA/A \approx 0.007\% \) (rms), ✔
- \( d\Phi \approx 0.004 \) deg at cavity bandwidth

Session 4: M.Hoffmann
„Single Cavity RF controls based on MTCA.4“
Laser Synchronization at REGAE in MTCA.4

- 3 GHz harmonic of laser extracted from Photo Diode → down converted to 25 MHz
- Phase noise measurement shows synchronization lock in the order of 20 fs

SSB Phase Noise:

~ 20 fs relative jitter reference (green) vs. laser (red)

Courtesy of M. Felber, U. Mavric
Signal Conditioning and Digital Processing

- High frequency Down-Converter (DRTM-DWC10)
  - 10 channel field detection
    (1.3GHz, …, 3.9GHz)
  - Resolution, 0.003%, 0.003deg, < 10fs

- Multi-Channel fast ADC Digitizer (SIS8300)
  - 10 channel ADCs (125Msps, 16-Bits)
  - FPGA pre-processing partial cavity vector sum
  - Low latency links via MTCA-backplane
Single channel performance in MTCA.4

> Short-term stability in an MTCA.4 crate (laboratory):

Test configuration:
- DWC8300 R1.0, SIS8300_V2, MCH, CPU, MTCA.4 crate
- DRO 1.3GHz (PSI), 1354 MHz LO, 54MHz IF, 81MHz SR
- LO-Generation Module (19”, FL, PM version)
- Offline Matlab non-iq analysis (N=65K), 1MHz Bandwidth

Power-Entry-Modules: < -110dB spurious free
Poor Power Supplies :  < -80dB SFDR
VS-Scaling        :  < -120dB SFDR

- Single cavity resolution of \( \Delta A/A = 2.8 \times 10^{-5} \) (<6 fs) is achieved
- Signal integrity in MTCA.4 crate achieved Eval board performance.
- Low distortion MTCA.4 power supplies.
- Guidelines for AMC and RTM designers (Grounding, power-supply, return-currents).

Raw-Data IF Spectrum (RF-signal off)

No bus traffic visible!

\( \Delta A/A = 0.0028\% \)
\( \Delta P/P = 0.004\° \)
Single channel performance in MTCA.4 at SLAC

ADC noise measurement:

SIS8900 – SIS8300

Comparative to datasheet SNR=78.2 dBFS

Signal to Noise Ratio (dBFS)

<table>
<thead>
<tr>
<th>ADC9</th>
<th>ADC1</th>
<th>ADC2</th>
<th>ADC3</th>
<th>ADC4</th>
<th>ADC5</th>
<th>ADC6</th>
<th>ADC7</th>
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<td>78.2</td>
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Crosstalk Matrix (dB)

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<thead>
<tr>
<th>ADC9</th>
<th>ADC1</th>
<th>ADC2</th>
<th>ADC3</th>
<th>ADC4</th>
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Amplitude (dBFS)

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Session 2: Z. Geng
MicroTCA Developments for Low Level RF and BPM for LCLS-II at SLAC

Zheqiao Geng, MicroTCA LLRF

2012-12-10
RTM Signal Conditioning to digital Zone 3

DRTM-AD84:
- 8 channel 10 MSPS, 16-Bit ADC
- 4 channel 1 MSPS, 16-Bit DAC

ADC raw data spectrum:
- CW signal, 100kHz, 450mVpp + spurious from ADC
- ADC floor < 115dBc spurious free (no signal, input matched, only GND connection)

Zone 3 Digital Signal Transmission

RTM: DRTM-AD84 – AMC: DAMC2

Courtesy of R. Meyer
Simplified Cable Management

> Introduction of an optional RF-Backplane:

DRTM-LOG1300 : eRTM low jitter signal generation

Complicated cable management  ➔  LLRF RF-Backplane concept

Session 3: T.Rohlev
„uLOG-Carrier eRTM Module“
Simplified Cable Management

> Successful test of an RF-Backplane in 02/2012
  - Low-jitter high-frequency signal distribution (< 10fs)
  - Low-jitter ADC-clock signal distribution (<200fs)

Session 5: K.Czuba
"RF Backplane for MTCA.4 Based Control System"

Courtesy of K.Czuba
Summary and Outlook

➢ A LLRF concept based on the MTCA.4 platform is presented.

➢ Resources are shared within DESY, collaborators and industry.

➢ Beam energy stability measurements of 0.005% using the MTCA.4 platform fulfil the XFEL requirements.

➢ Low distortion power supplies are needed.

➢ A Crate, AMC, RTM module distortion classification is needed.

Thanks for your attention!