Beyond 10 Gbps
with
MTCA.4
Agenda

- Data Transport in MTCA.4
- Current Development
- Data Processing and Telecommunication Module
- MTCA.4 Chassis Evaluation
MTCA.4 provides three ways for data transmission:

- Zone 1 (backplane)
- Zone 3 (RTM)
- Front-panel

MTCA Zone 1 connector divided into zones:

- Star connection on ports 0 and 1
- P2P connection on ports 2 and 3
- Star connection via switch on ports 4-7
- Star connection or P2P on ports 8-11
- P2P connection on ports 12-15
Data Transport in MTCA.4 (2)

- **MTCA.0** defines support for up to 12.5 Gbps
- **AMC.1 AdvancedMC™ PCI Express and AS**
  - Single and Quad channel
  - PCIe gen. 1 (2.5 Gbps/channel)
  - PCIe gen. 2 (5 Gbps/channel)
  - PCIe gen. 3 (8 Gbps/channel)
- **AMC.2 AdvancedMC™ Ethernet:**
  - 1000Base-BX
  - 10GBase-BX4
- **AMC.3 AdvancedMC™ Storage**
  - SATA, SAS, Fiber Channel
- **AMC.4 AdvancedMC™ Serial RapidIO**
  - 1.25, 2.5, 3.125 Gbaud
  - Single or Quad channel
Data Transport – Current Development

- PICMG, Higher Speed Ethernet Working Group (HSEWG)

- Develop enumerated requirements for MTCA.0 and AMC. 2 supporting:
  - 10GBASE-KX4
  - 10GBASE-KR
  - 40GBASE-KR4
  - Common Option (ports 0 and 1)
  - Fat Pipes (ports 4-7)
  - Extended Pipes (ports 8-11)
  - Keep backward compatibility with existing MTCA.x and AMC.x spec.

- 10 Gbps backplane required
DAMC-TCK7 – Data Processing and Telecommunication Module

Features:

- Xilinx Kintex 7 XC7K355T/XC7K420T FPGA
- SDRAM: 16 Gb DDR3 SDRAM@533 MHz
- **Connectivity:**
  - 24 or 28 gigalinks, baudrate max. 12.5 Gbps
  - PCIe x4, gen. 3 (32 Gbps)
- **Low-latency links:**
  - Backplane: 10x 10 Gbps
  - Front panel: 8x 12.5 Gbps (SFP+)
  - Zone 3: D1.2 Digital Class (4x 12.5 Gbps)
- Flexible clock distribution and synchronization
- IPMI management and diagnostics
- FPGA firmware upgrade support
- Funded by the HVF "MTCA.4 for Industry"
Beyond 10 Gbps with MTCA.4

DAMC-TCK7 – Data Transport

Front-panel
- 4x SFP+ (12.5 Gbps)

Backplane
- 2x 1000Base-BX (1 Gbps)
- 2x P2P (10 Gbps)
- PCIe x4 gen. 3 (8 Gbps)
- 8x P2P (10 Gbps)

Zone 3
- 4x P2P (10 Gbps)

Kintex 7 XC7K355T
Test Procedure

- The aim:
  Test and understand the limitations of currently available MTCA.4 hardware

- Hardware used during test:
  - 3 different MTCA.4 chassis
  - MCH
  - CPU
  - Endpoint device (4x DAMC-TCK7), PLDA PCIe x4, gen. 3 endpoint

- Test of available interfaces:
  - PCIe gen. 3
  - Peer-2-Peer links (>8 Gbps)
  - 10/40 GbE
Hardware Used During Tests
Peer-to-Peer Connectivity

- Direct connection between ports on the same card
- Connection between two modules
- Clock generated locally (f=125 Mhz)
- Xilinx IBERT program used for BER evaluation
- Custom Low-latency protocol
- Short and long-term tests
Switched Data Transfer - PCIe

Beyond 10 Gbps with MTCA.4

Switched Data Transfer - PCIe

CPU
PCle x4/3

MCH
NAT-MCH-PHYS

Concurrent
AM914/412
Results of Evaluation

MTCA.4 chassis – vendor 1 (LLRF backplane)
- PCIe: links negotiated with gen. 3
- P2P (ports 2-3): 10 Gbps BER: $\sim 10^{-13} \text{ bit}^{-1}$
- P2P (ports 8-15): 10 Gbps $< 10^{-14} \text{ bit}^{-1}$ (limited by test time)

MTCA.4 chassis – vendor 2 (LLRF backplane)
- PCIe: links negotiated with gen. 3
- P2P (ports 2-3): 10 Gbps $\sim 10^{-4} \text{ bit}^{-1}$
- P2P (ports 8-15): 10 Gbps $10^{-14} \text{ bit}^{-1} - 10^{-6} \text{ bit}^{-1}$

MTCA.4 chassis – vendor 3 (PICMG backplane)
- PCIe: links negotiated with gen. 1
- P2P (ports 2-3): 10 Gbps $\sim 10^{-4} \text{ bit}^{-1}$
- P2P (ports 8-15): 10 Gbps $10^{-11} \text{ bit}^{-1} - 10^{-5} \text{ bit}^{-1}$
Summary

- MTCA.4 chassis from 3 vendors were tested
- PCIe:
  - Two chassis works with PCIe gen. 3
  - One is limited to PCIe gen. 1
- P2P channels:
  - One chassis works with 10 Gbps
  - One works with 3.6 Gbps
  - One works with 4 Gbps
- Common Region not tested:
  - Not tested with >1 Gbps
  - Backplane ?
  - CPU ?
  - MCH ?
Thank you for your attention